# DEVELOPMENT OF SYSTEM LEVEL INTEGRATION OF COMPACT RF COMPONENTS ON MULTILAYER LIQUID CRYSTAL POLYMER (LCP)

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# DEVELOPMENT OF SYSTEM LEVEL INTEGRATION OF COMPACT RF COMPONENTS ON MULTILAYER LIQUID CRYSTAL POLYMER (LCP)

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| | |
|---|---|
| 3D | Three Dimensional |
| AiP | Antenna-in-Package |
| AoC | Antenna-on-Chip |
| CBCPW | Conductor Backed Coplanar Waveguides |
| CPW | Coplanar Waveguides |
| CTE | Coefficient of Thermal Expansion |
| DC | Direct Current |
| DI | De-Ionized |
| DUT | Device Under Test |
| EM | Electro-Magnetic |
| FCC | Federal Communications Commission |
| FET | Field-Effect Transistor |
| FR-4 | Flame Retardant 4 |
| GCPW | Grounded Coplanar Waveguides |
| GPS | Global Positioning System |
| HDI | High Density Interconnects |
| HF | Hydrofluoric |
| IC | Integrated Circuits |
| IEEE | Institute of Electrical and Electronics Engineers |
| IPA | Isopropyl Alcohol |
| ISM | Industrial Scientific Medical |
| LCP | Liquid Crystal Polymer |

| | |
|---|---|
| LOS | Line of Sight |
| LTCC | Low Temperature Co-fired Ceramic |
| LTE | Long Term Evolution |
| MCM | Multi-Chip Module |
| MEMS | Micro-Electro-Mechanical Systems |
| MIMO | Multi Input Multi Out put |
| MLO | Multi-Layer Organic |
| NASA | National Aeronautics and Space Administration |
| PA | Power Amplifier |
| PCB | Printed Circuit Board |
| PECVD | Plasma-Enhanced Chemical Vapor Deposition |
| PIN | P-type Intrinsic N-type |
| PGMEA | Propylene Glycol Monomethyl Ether Acetate |
| PTFE | Polytetrafluroethylene |
| PZT | Lead Zirconate Titanate |
| RIE | Reactive Ion Etch |
| RF | Radio Frequency |
| RPM | Rounds Per Minute |
| SP2T | Single Pole Double Throw |
| SP3T | Single Pole Three Throw |
| SP4T | Single Pole Four Throw |
| SiP | System-in-Package |
| SLL | Side Lobe Level |
| SOLT | Short Open Load Through |
| SOP | System-On-Package |

| | |
|---|---|
| TTD | True Time Delay |
| V-band | 55 – 75 GHz |
| W-band | 75 – 110 GHz |
| WLAN | Wireless Area Network |
| X-band | 8 – 12 GHz |

# SUMMARY

The objective of this research is to optimize compactness for reconfigurable wireless communication systems by integrating Radio Frequency (RF) components on a multilayer Liquid Crystal Polymer (LCP) package while minimizing the size and interconnection of each component. To achieve this goal, various RF/microwave components have been integrated on LCP with the design, fabrication, and testing results to explore the feasibility of the designs for RF applications.

The first chapter of this research focuses on the characterization of via interconnects for 3D system designs. As a crucial component for achieving compact multilayer designs, various transition designs are explored from DC to 110 GHz. In particular, High Density Interconnects (HDI) are investigated to achieve low loss performance at mm-wave frequencies. An example of accessing the input and output of a LCP packaged device using via interconnects is included. In addition, a heat sink using via technology is presented for active cooling of heat generating embedded devices.

Chapters 3, 4, and 5 demonstrate the results of RF Micro-Electro-Mechanical Systems (MEMS) switches integrated on LCP to create compact reconfigurable devices. RF MEMS switches are essential for designing compact multi-functional devices. A pattern reconfigurable antenna with monolithically integrated RF MEMS switches is presented. In addition, a compact 3D phase shifter using RF MEMS switches for a 2 x 2 phased antenna array is also presented in this work. To create a phased antenna array that is more compatible with Integrated Circuits (IC), Lead Zirconate Titanate (PZT) RF MEMS switches are used to make a low voltage phase shifter. The actuation voltage is under 10 V, which is more easily achievable in a integrated system compared to commonly used electrostatic actuated RF MEMS switches that required at least 30 V.

In Chapter 6, an expandable, low cost, and conformal multilayer phased antenna array is presented. Starting with a 4 x 8 element antenna array, the concept of beam steering is shown. Using this antenna array as a building block, an 8 x 8 element antenna array is shown with the measured results when conformed around a cylinder. Further expanding the antenna array, a 16 x 16 element antenna array is designed, fabricated, and measured. All of these antenna arrays use LCP as a platform for lightweight and low cost satellite communication applications.

Finally, using the integration technology and expertise developed from the previous work, a 60 GHz transceiver front end is designed on LCP for high speed wireless communication applications. Two dual mode filters and high-gain vertical dipoles are integrated at the packaging level on LCP to create a low cost system. A PA and LNA are included in the system to increase the system gain. The measurements of the dual mode filters are presented as well as the fully integrated transceiver pattern measurements and gain measurements of each of the transmitting and receiving mode.

This research contributes to LCP integration technology with more compact and higher frequency multilayer applications while focusing on integration of the components at the system packaging level to achieve optimal compactness. The highlight of this work is in developing key technologies for multilayer integration on organic LCP such as HDI interconnects and RF MEMS; applying the technology to create reconfigurable RF components such as reconfigurable antennas and compact low voltage phase shifters; and integrating the components to create compact low cost multilayer RF front end systems.

# CHAPTER 1

# INTRODUCTION

## 1.1 Background on Wireless Communication and Multilayer Integration

Our daily lives have evolved over the past century with the introduction of wireless technology as it has allowed people all over the world to share information and communicate with each other at the tip of their hand. Every part of our lives is dependent on wireless technology at work, at home, on vacation, and even for socializing. A few examples of wireless devices that have become a vital part of our lives are:

- Radio and TV broadcasting along with the remote control
- Cellular phones and smart phones
- Satellite navigation such as Global Positioning System (GPS)
- Wireless networks such as Wi-Fi, Bluetooth, and WLAN
- Air traffic control and transportation sensor networks
- Weather monitoring and forecasting
- Military defense including missile guidance systems and missile defense
- Sensor networks
- Radars and remote sensing.

As new technologies emerge, the applications and market for wireless devices and system have continuously expanded. The size of the wireless market has grown to over $150 billion in the US alone and over $1.1 trillion globally with over 5 billion subscribers for mobile devices [1], [2]. In addition, the US Department of Defense has invested over $1.5 billion in missile defense and over $3 billion for NASA and satellites in the year 2010 [3], [4]. The demand for smaller and functionally more powerful devices is

increasing as the applications and communication market continually grow, saturating the existing frequency bands. To overcome the crowding of the limited bandwidth in the commercial wireless communication bands, the market has aimed towards higher frequency bands as well as employing Multi-Input Multi-Output (MIMO) technologies. The Shannon-Hartley theorem states that the channel capacity increases with larger channel bandwidth and signal-to-noise ratio. There is larger available channel bandwidth at higher frequencies, such as the 60 GHz unlicensed band, while more compact structures are realizable with shorter effective wavelengths. The lower frequency bands below 10 GHz are crowded with numerous applications and have limited bandwidth availability. For example, at the Industrial, Scientific, Medical (ISM) band at 2.4 GHz, the channel bandwidth is 22 MHz, yielding a maximum data rate of 54 Mb/s with IEEE 802.11g standard. However, the 60 GHz band allows 2.16 GHz channel bandwidth and ideally, multi-giga bits per second is achievable. Meanwhile, within the existing crowded low frequency bands, the early pioneering work by Foschini and Telatar shows that MIMO systems greatly increase the system capacity over a shared bandwidth [5], [6]. In the ISM band, a 2 x 2 MIMO system using IEEE LTE standards achieves up to 360 Mb/s while IEEE 802.11n standard reports a 4 x 4 MIMO system to reach 600 Mb/s with 40 MHz bandwidth [7], [8]. Additionally, commercial products that use 2 x 2 MIMO systems report up to 300 Mb/s through put.

As wireless communication technologies evolve, the networks and devices have become increasingly more complex and the number of RF components in a given real estate has increased drastically. However, the trend for handheld mobile devices as well as communication systems in extreme environments requires low power, compact, and highly functional systems. Thus, with more components but less real estate, RF and microwave engineers are compelled to explore enabling technologies to create lightweight, compact, and multifunctional wireless components.

One approach to creating multifunctional but lightweight and compact devices is to reduce the bulky footprint and weight at the system packaging level, also known as System-On-Package (SOP). Taking the advantages of Multi-Chip Module (MCM), which interconnects multiple components in two dimensions, and System-in-Package (SiP), which packages IC chips in three dimensions, the SOP approach offers maximum compactness for multifunctional devices [9] – [11]. An example of a SOP package is shown in Figure 1. Flip chip technology is used to minimize the interconnect length for the IC chips. With shorter interconnects, higher efficiency is achieved in the system with reduced power consumption, delay, and noise. Passive components such as resistors and capacitors are integrated directly using thin film technology to avoid bulky individual packaging. Filters, phase shifters, and other devices are integrated through IC chips or included at the packaging level. An antenna or an antenna array is at the end of the system for transmitting and receiving signals. The multilayer stack up allows embedded grounds for higher isolation between components and to significantly reduce the overall size. Embedded cavities are used to provide hermetic seals for moisture sensitive devices such as RF MEMS and unpackaged IC chips. Digital control lines are routed in the stack up for the overall control of the system. Finally, thermal vias are included for passive or active thermal management, which is crucial for multilayer systems to avoid catastrophic failure. The advantages of SOP allow existing technologies, such as SiP and MCM, to be easily integrated on the packaging platform while the multilayer stack up reduces the overall layout area. With lines routed on different layers, each layer is less crowded and greater isolation is achieved in a dense area. Thus, an SOP approach to system integration offers a compact multi-functional solution for high performance future applications.

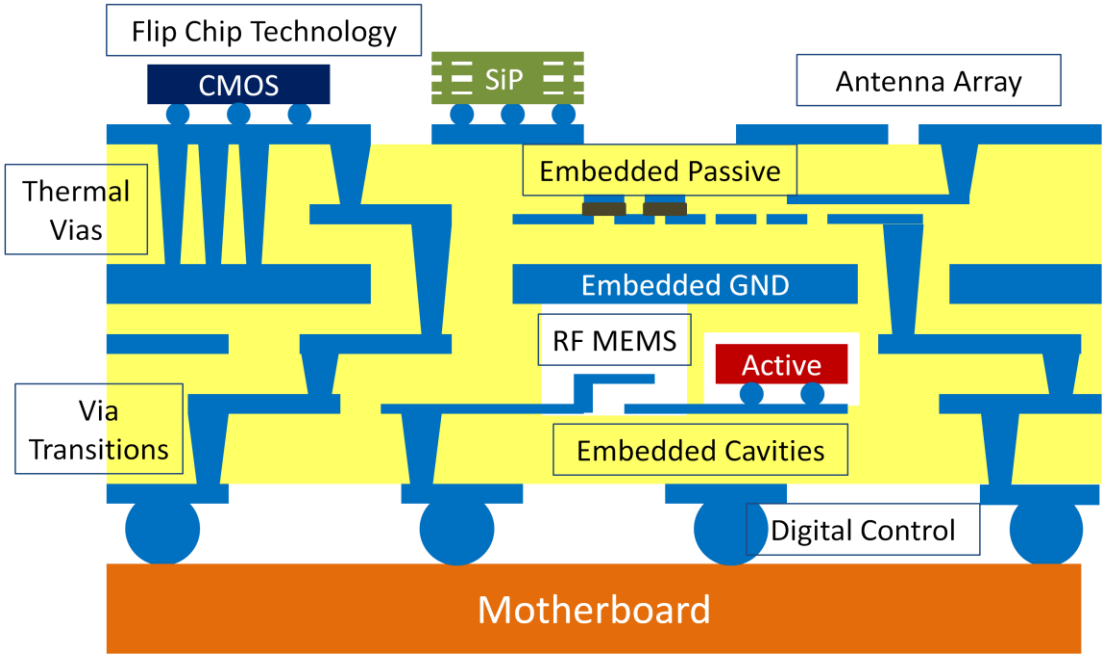



Figure 1: Cross sectional view of a SOP system example.

## 1.2 Background of Multilayer Integration on LCP

To maximize the advantage of SOP for a lightweight multi-functional system, a low cost lightweight substrate with multilayer processing capabilities must be selected. Table 1 shows a comparison of the material properties of commonly used high frequency materials. Flame Retardant 4 (FR-4) is an epoxy based substrate that is cheap, light, and the most commonly used material for Printed Circuit Boards (PCB). However, the material is lossy and not suitable for high frequency applications above 10 GHz. Polytetrafluroethylene (PTFE) is a chemically inert polymer that has excellent RF properties but the Coefficient of Thermal Expansion (CTE) is high, which causes de-lamination of metals over thermal cycles, and multilayer processing is difficult. Low Temperature Co-fired Ceramic (LTCC) also offers great electrical properties, and as a result, LTCC is commonly used for high frequency multilayer stack ups. The drawback of LTCC is that it is expensive and heavier compared to the other high frequency materials. In addition, the firing temperature of 850 $^{o}$C is too high for most IC devices

Table 1. Material comparison for high frequency circuits

| | FR-4[12],[13] | PTFE[14],[15] | LTCC[16] –[19] | LCP[19] |
|---|---|---|---|---|
| Dielectric Constant ($\varepsilon_r$)* | 3.8 – 4.3 | 1.92 – 2.33 | 5.9 - 9 | 2.9 |
| Loss Tangent ($\delta$)* | 0.016 | 0.0003 – 0.0011 | 0.001 | 0.0025 |
| CTE (ppm/$^o$C) | 12 - 17 | 25 - 80 | 4.4 - 7 | 17 |
| Processing Temp. ($^o$C) | < 425 | < 285 | 850 | < 300 |
| Density (g/cm$^3$) | 1.85 | 2.23 | 3.1 | 1.4 |

* Measured at 10 GHz

limiting the possibilities of embedding devices.

LCP has RF electrical properties comparable to PTFE and LTCC. The high frequency characteristics have been well documented, showing a loss tangent of 0.004 at 60 GHz and 0.0045 at 97 GHz as well as a stable dielectric constant with less than 5% variation from DC to mm-wave frequencies [20], [21]. The CTE of LCP matches exactly to the most commonly used copper and can be manufactured to have a CTE anywhere from 2 to 30. This is important because a CTE offset causes delamination of materials over thermal cycles. LCP is considerably lighter than other commonly used RF substrates as well. LCP is 25 % lighter than FR-4 and 40 % lighter than silicon. The processing temperature of LCP is below 300 $^o$C, as a LCP bond ply material that melts at 285 $^o$C but exhibits the same electrical properties, allowing uniform multilayer processing. The high melt material has a melting temperature of 315 $^o$C, which opens up a temperature window for processing. Standard multilayer PCB processing of large panels (12 inch x 18 inch or larger) is applicable for LCP. A diverse number of thickness starting from 1 mil of LCP is available that allows a multilayer stack up to reach almost any thickness. The challenges with multilayer processing on LCP are the thickness variation in the material

that is reported at 12.5 % as well as the shifting of metal during the lamination processes. These problems are overcome by accounting for the thickness variations and misalignments in the simulations. The large panel processing increases the number of component output that drives the price of an individual component down. In addition, LCP is near hermetic, chemically inert, and radiation resistant, making it a great packaging material. The bond ply adheres to most substrates to create a hybrid integrated package. The large processing and packaging capabilities of LCP enables a lightweight low cost SOP platform for RF systems. Thus, with many promising attributes as a high frequency substrate, LCP is selected as the core material in this thesis.

As many via transitions are seen in Figure 1, via transitions are an essential technology for multilayer processing. Via transitions allow direct access from one layer to another in a minimal space and very low loss. Compared to via-less transitions [24], [25] via transitions give wideband performance, higher isolation, and minimal required space. Therefore, it is important to study the performance of via transitions on multilayer LCP as this thesis focuses on compact 3D structures. In addition, vias are used for thermal management of a system when integrating heat generating active circuitry such as a Power Amplifier (PA). Since LCP is an organic material, it has a low thermal conductivity and the heat generated from the devices cannot dissipate fast enough without proper thermal management, resulting in overheating of the system that leads to poor efficiency in performance and ultimately to failure of the system. Since LCP is a poor thermal conductor as any other organic material, thermal management is a high priority issue to address in a multilayer system. Therefore, an active cooling system using thermal vias is investigated in this thesis as well.

## 1.3 Background on RF MEMS

RF switches for multifunctional devices are commonly made with Field Effective Transistor (FET) switches, PIN diodes, or RF MEMS switches. At low frequencies, FET

switches and PIN diodes are cheaper and are easy to integrate as a component. However, as the frequencies increase, parasitic effects complicate the design and designing a good compact biasing network becomes a challenge. In general, RF MEMS devices offer the following advantages over traditional GaAs FETs and PIN diodes:

- Near-zero power consumption
- High linearity
- Low loss
- High Isolation
- Wideband performance.

Various actuation mechanisms are used to actuate RF MEMS, each with its own advantages and disadvantages compared to its counterparts. The tradeoff of the actuation types is a decision for the RF designer to make for the specific application. Electrostatic actuation is the most commonly used actuation method that gives the fastest switching speed in the range of a couple μs and requires the least area. However, the actuation voltage is relatively high in the range of 30 – 100 V. This high voltage becomes a challenge for system level integration, particularly for integrating active components, which typically operated below 5.5 V. The main failure mechanisms, dielectric charging and mechanical wear, cause degradation of the performance of the switch. Thermal actuation allows low actuation voltage and higher reliability compared to electrostatic actuation, as thermal actuation does not have to deal with dielectric charging. Additionally, a high contact force is achievable for less contact resistance, but the overall size is relatively large, the switching speed is slow, and the power consumption is not zero. Magnetostatic actuation has similar characteristics as thermal actuation with low voltage and higher reliability but it displays slow speed and higher power consumption. The power consumption problem can be resolved by creating a hybrid electro-thermal actuation for the thermal actuation or by using permanent magnets for the magnetostatic

actuation. Piezoelectric actuation has low voltage actuation compared to electrostatic actuation but higher than the thermal or magnetostatic actuation. The power consumption is near zero, but the switching speed is slower and the size is bigger than the electrostatic actuation.

Another way to categorize RF MEMS switches is by the contact type. The two types are the direct (or ohmic) contact, which uses metal to metal contact when actuated, and capacitive contact, which has a thin dielectric in between the metal surfaces. The direct contact switches operate at DC – 60 GHz and capacitive switches operate at 10 – 120 GHz [26]. The main challenges in designing the ohmic switches are to increase the contact force for lower contact resistance while avoiding wearing of the contact surface. On the other hand, dielectric charging is the main challenge for capacitive switches while achieving a high on-off capacitance ratio.

Traditionally, RF MEMS switches have been built on silicon or other solid surfaces, but for integration purposes, a recipe has been developed to build directly on flexible organic LCP [27], [28]. Though there are more variables to consider in developing this recipe, in general, the process uses standard MEMS fabrication steps that do not incur additional cost. A selected number of papers show monolithically integrated RF MEMS switches on LCP to create reconfigurable devices [29] – [31]. By monolithically integrating RF MEMS switches on LCP, two main advantages of reduced loss and a more compact device is achieved. A higher efficiency is achieved with monolithic integration where interconnects between the MEMS switch and the adjacent component are avoided. The interconnects add parasitic effects that degrade the overall performance, and therefore, avoiding or reducing the length of the interconnects is beneficial for the system. In addition, by avoiding or reducing the length of interconnects, the overall size is reduced with minimal area needed for integrating a switch as a monolithically integrated RF MEMS switch is able to fit in gaps below 100 μm.

Monolithic integration also improves the overall matching especially at higher frequencies and when narrow lines are used on thin substrates.

In this thesis, electrostatic capacitive MEMS switches are monolithically integrated on multilayer LCP to create a reconfigurable antenna. In addition, for lower actuation voltage and better integration compatibility, piezoelectric ohmic MEMS switches are used to create a compact phase shifter.

## 1.4 Phased Antenna Arrays on LCP

Phased antenna arrays are of great interest for various communication systems that require scanning of narrow directive beams including satellite communications, military radars, weather monitoring systems, broadcasting, and space-based radars. Phased antenna arrays also benefit MIMO systems in creating smaller and more compact systems. As mentioned in Chapter 1.1, MIMO systems have attract much attention as they provide increased channel capacity for the crowded and limited communication bands. Research shows that directional antennas provide more system capacity with the trade off of complexity [32], [33]. Antenna arrays produce narrower radiation patterns with high directivity. However, a simple passive antenna array points a narrow beam in one direction, which makes it difficult to realize communication between multiple inputs and outputs. Using passive antenna arrays to create a working MIMO system would require additional antenna arrays and each would have to be separated several wavelengths apart for isolation. High isolation is needed in MIMO systems as the isolation reduces the correlation between the channels resulting in lower error. The use of additional antenna arrays creates a heavy, complex, and large system that is undesirable. To overcome these problems, phase antenna arrays have been studied for MIMO systems [34]. Phased antenna arrays allow a single antenna array to steer the beam in multiple directions. This allows avoiding additional antenna arrays and reduces the overall size,

weight, and complexity. Thus, phased antenna arrays provide an advantage for MIMO systems that is essential for the growing communication industry.

In theory, the 3-dB beam width of an antenna is directly related to the resolution capability of an antenna to distinguish between two targets [35]. Since a narrower beam is acquired by having more array elements, the size of the antenna array becomes fairly large for high resolution applications. With large antenna arrays, the weight, cost, and loss are important factors in designing the array. LCP as a substrate provides an advantage over other materials in these aspects. The substrate is approximately 25% lighter than FR-4, cheaper than LTCC and are processed in large panels (12 in x 18 in and larger), which is not available for Duroid material.

Phased antenna arrays are reconfigurable antenna arrays that have the ability to scan the beam with given phase differences to the array elements. The phase shifters that allow electronic control of the phase shift are typically ferrite or diode phase shifters [36]. Ferrite phase shifters generally offer the advantages of high power handling capability and low cost compared to diode phase shifters. The typical principle of operation is by changing a bias field on a ferrite material, which in turn changes the electrical properties of a transmission line to provide a phase shift. However, ferrite based phase shifters suffer from being bulky, lossy and hard to integrate compared to diode phase shifters. Diode phase shifters on the other hand are easier to integrate, smaller, and operate at a higher speed. There are three types of diode phase shifter designs, which are a switched line, loaded line, and reflection type phase shifter [36]. The switch line phase shifter is the simplest design with delay lines for each phase state. Loaded line phase shifters use shunt loads that are modeled in the equivalent circuit as a section of transmission line with a characteristic impedance and length that are both dependant on the loads. Finally, the reflection type phase shifter uses diodes to create a short along a transmission line for reflections at different points along that allows varying phase shifts. The reflection type phase shifter uses hybrids, circulators, or couplers to provide a two-port circuit [36].

Despite the advantages of the diode phase shifters, at higher frequencies, the bias networks become large and harder to design and integrate. The biasing network contributes to the increasing loss as well as the loss inherent to the device. With increasing number of components, power consumption of the diode switches are a potential problem for large arrays.

As RF MEMS provide advantages of high isolation, low loss, and near zero power consumption compared to diode switches at high frequencies, RF MEMS phase shifters have been extensively researched [28], [37] – [39]. There are three main types of MEMS phase shifters, which are switched line, distributed, and reflection type. The switched line phase shifter is also called a delay line or True Time Delay (TTD) phase shifter. As mentioned before, it is the most straight forward design that typically uses Single Pole Double Throw (SP2T) junctions [40], while an effort has been made for using Single Pole Four Throw (SP4T) junctions to reduce the footprint [28], [37]. The distributed line phase shifter uses RF MEMS switches to vary the distributed capacitance on a transmission line that changes the phase velocity of the line [41]. The reflection type is the same concept as the diode reflection type phase shifter. Both the distributed and reflection type phase shifters add more loss and are larger than the switched line phase shifter. In general, most RF MEMS phase shifters use electrostatically actuated RF MEMS switches that require a voltage in the range of 30 – 100 V, which is a relatively large voltage for integrating with other RF front end components. Typical IC chips operate below 5.5 V; to achieve the voltage required by the electrostatic actuated RF MEMS switches, additional components and biasing networks are needed along with separation for high isolation. To overcome the high voltage for integration, piezoelectric MEMS switches that actuate as low as 2 V have been developed [42], [43]. In this thesis, the low voltage piezoelectric MEMS switches are used to create a compact 3D phase shifter for phased array applications.

This thesis includes a conceptual study of a reconfigurable, lightweight, and flexible phased antenna array on multilayer LCP for deployable satellite communication applications. Using the multilayer capabilities of LCP, an expandable antenna array is designed for future large antenna array applications. The unit array includes a monolithically integrated phase shifter as a proof of concept.

## 1.5 mm-Wave Wireless Communication Modules on LCP

The recent advances in wireless technology and consumer electronics have led the interest of the wireless community to the 60 GHz band for ultra-high speed data transfer in short range communication. In the United States of America, the Federal Communication Commission (FCC) has allocated the band of 57 – 64 GHz for the general public. The near 9 GHz spectrum of 57.24 – 65.88 GHz, which covers all the unlicensed 60 GHz bands worldwide, promises multi-giga bit per second data rate and highly secure communication with minimal interference due to the high atmospheric attenuation [44], [45].

System level integration has been a focus of many researchers at the 60 GHz band frequencies as design and integration at these frequencies pose difficult challenges due to high loss and increased frequency dependent parasitic effects. In particular, realizing a 60 GHz transceiver front end requires an optimal system level integration as the packing material and performance of each RF component as well as interconnects affect the overall performance of the system. Antenna-on-Chip (AoC) and Antenna-in-Package (AiP) are the two main approaches for designing mm-wave transceivers as the antenna affects the overall design of the system [46]. The AoC approach allows compact integration but has limited performance with typically negative gain antennas [45] – [47].

Improving the performance requires non-standard processes that increase the overall cost and complexity of fabrication. The AiP technology for 60 GHz radio has a clear advantage with higher efficiency antennas built on low loss materials [46], [48] – [50]. The package level integration can be expanded to include additional RF passive components to avoid the individual packaging, decrease the interconnect lengths, and further reduce the overall cost, which is the SOP concept. LTCC is the most widely used substrate for SOP applications with superior performance and multilayer stack ups but at a higher cost and limited integration capabilities due to the high firing temperature (850 $^{o}$C) [51] – [53]. A low cost lightweight alternative liquid crystal polymer (LCP) has emerged as a promising packaging material that has excellent electrical and mechanical properties. A 60 GHz transmitter using multilayer organic (MLO) LCP has been reported in [49] with comparable results to LTCC but at a lower cost and better integration capabilities with processing temperature below 300 $^{o}$C. In addition, a similar 60 GHz transceiver front end is presented in [54], but it is a single layer design and simultaneous communication is not available because of the use of a switch. In this thesis, a 60 GHz transceiver front end is integrated on MLO LCP for low cost wireless communication systems.

## 1.6 Contributions and Organization

In this dissertation, we have explored various high frequency wireless communication applications with system level integration technology. The use of LCP allowed the design of low cost, lightweight, and compact multilayer systems. The contributions of this thesis are in the design and integration of low voltage and compact RF components and technology at the system packaging level for optimal efficiency.

Chapter 2 focuses on via technology to demonstrate the first V-band and W-band HDI via transitions on LCP and LCP/Si hybrids. In addition, the first low cost active cooling system on LCP/Si hybrid is demonstrated with a micro pump for thermal management on a compact multilayer stack up.

In Chapter 3, the MEMS process of monolithically integrated RF MEMS switch on LCP is presented. Using these RF MEMS switches, the first monolithically integrated pattern reconfigurable antenna on LCP is presented for MIMO military applications.

In Chapter 4, a compact 3D phase shifter using commercially available SP4T RF MEMS switches is presented on LCP for the first time. Using these phase shifters, a 2 x 2 element patch array with beam steering capability is demonstrated on multilayer LCP.

Chapter 5 presents low voltage PZT RF MEMS SPDT and SP4T switches for improved integration capabilities. A compact PZT RF MEMS 3D phase shifter with the SP4T switches integrated on multilayer LCP is presented for the first time.

In Chapter 6, expandable phased antenna arrays on multilayer LCP have been demonstrated up to 256 elements for the first time. The beam steering of the phase arrays have been demonstrated as well as flexibility of LCP for conformal applications.

In Chapter 7, a 60 GHz transceiver front end with simultaneous transmitting and receiving modes have been shown on multilayer LCP for the first time. The proposed structure shows a low cost solution for 60 GHz wireless applications. A higher isolation between the two modes is achieved with orthogonal polarization of the two modes.

Chapter 8 summarizes the work with a conclusion and contributions.

# CHAPTER 2

# VIA TECHNOLOGY

Via transitions, or vertical transitions, are essential for multilayer processing as they offer low loss, wideband performance, and most importantly direct access from layer to layer in minimal area. In particular, small vias (less than 100 μm diameter), known as HDIs, are needed to minimize the parasitic effects as the frequency increases. Another option is to use coupled line transitions to access another layer. However, via-less transitions have limited bandwidth, they are complicated to design, and the signal can easily couple over to unwanted areas so that to maintain the same isolation level, a large spacing is required [24], [25]. In this chapter, low loss vertical transitions are presented from DC to 110 GHz on multilayer LCP. Vertical transitions on a homogenous substrate (RO4003 – hydrocarbon ceramic material) have been made with excellent performance from DC to 60 GHz [55]. Similar via transitions on a single layer LCP has been shown [56]. The work in this thesis improves on the existing work with reduced loss and better performance over a wideband frequency. The size of the via is smaller for direct access to embedded IC chips. In addition, vertical transitions on LCP laminated to Si are investigated to emulate transitions on embedded devices, which are commonly high dielectric substrates.

Via technology is also helpful for thermal management in multilayer systems with embedded components. The biggest challenge in embedding communication components is the heat generated from high power components such as a PA in the transmitter. Thermal vias assist in transferring the heat, which is critical to multilayer integration as LCP and other organic substrates are poor thermal conductors. An active cooling system concept for a multi-substrate application is also discussed in the chapter.

## 2.1 Via modeling

A via transition is simply modeled by a series inductance ($L_v$), resistance ($R_v$), and parallel capacitance ($C_t$ from the top, $C_b$ from the bottom) as shown in Figure 2. The effective impedance of a via is divided into the real part and imaginary part. The real part is affected by the resistance $R_v$ that causes the via to have more loss with increasing resistance. The imaginary part is affected by the inductance $L_v$ and capacitance $C_t$ and $C_b$ where for a perfect match with the line impedance, the effects need to cancel each other. This process is optimized most easily with a 3D Electro-Magnetic (EM) simulation tool, such as Ansoft HFSS or CST Microwave Studio. Typically, the smaller the via diameter and the longer the via is, the inductance and resistance increases. In addition, the electrical length of the via increases with increasing frequencies, and therefore, the inductance and resistance increases with frequency. The capacitance is affected by the signal to the ground distance. The further the distance the less capacitance in the same sense as a capacitor. The landing pads of the via, which are extra area around the via to ensure a connection even with misalignment, are the main contributors to the parasitic capacitance. Figure 3 shows the side view of (a) via transitions through a single layer and (b) through an embedded ground. In a simple model, the transition going through an embedded ground has additional capacitance $C_v$ that needs to be taken into consideration in the simulation. This is done by cutting back the embedded ground around the via to

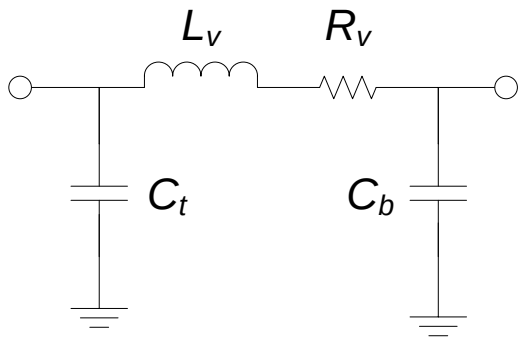
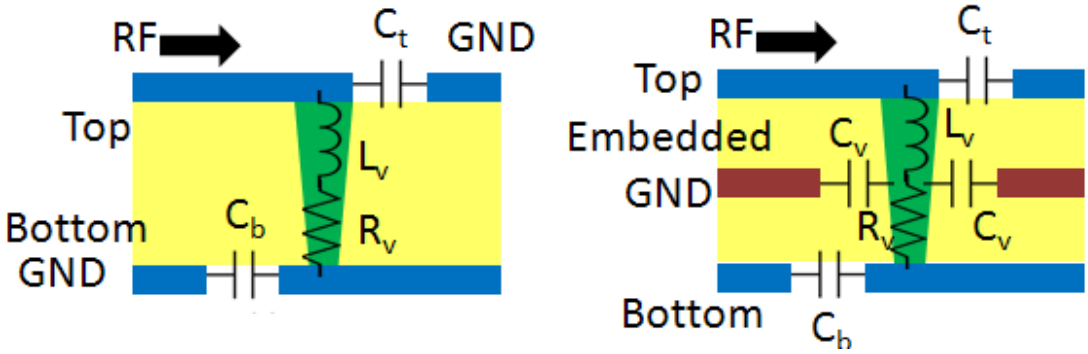


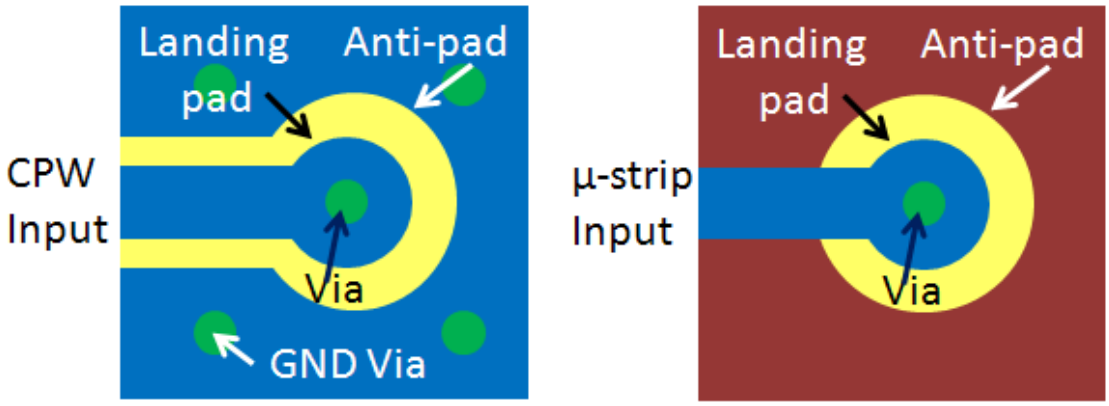

Figure 2: Equivalent model of a via transition.

reduce the capacitance and give access to the via, which is called an anti-pad as seen in Figure 4. Figure 4 (a) shows Coplanar Waveguide (CPW) via transition and Figure 4 (b) shows a microstrip via transition. The CPW transition has the anti-pads on the same level as the signal line as the ground plane is on the same layer. The microstrip via transition has the anti-pad embedded with the signal via going through the ground to the opposite side. Changing the size of the via changes the parasitic capacitance that has the greatest effect trying to optimize the transition.




(a) (b)

Figure 3: Side view of via transitions on (a) one layer and (b) through an embedded ground.




(a) (b)

Figure 4: Top view of (a) CPW via transition and (b) microstrip via transition.

## 2.2 3D via transitions

Conductor Backed Coplanar Waveguides (CBCPW), or Grounded Coplanar Waveguides (CPWG), are commonly used in RF and microwave circuits as they provide accessible common ground references for the entire circuit. In multilayer designs, the bottom ground plane is also used to isolate components and reduce the back side radiation. Despite these advantages, the CBCPW structure can easily excite undesirable excess modes at higher frequencies [57]. When the finite ground planes have open boundaries, the ground planes act as two patches fed by the slots of the CPW with a resonance governed by the following equation (1),

$$f_{mn} = \frac{c}{2\sqrt{\varepsilon_r}} \cdot \sqrt{\left(\frac{m}{W_g}\right)^2 + \left(\frac{n}{L_g}\right)^2} \quad , \tag{1}$$

where $\varepsilon_r$ is the relative dielectric constant, $m$ and $n$ are integers of the modes, and $W_g$ and $L_g$ are the dimensions of the ground plane. By placing vias in the positions where the $E$-field is at its maximum can reduce these excess modes [58]. Thus, it is necessary to place vias as close to the edges of the ground planes as shown in Figure 5 (a). To verify the effectiveness of via transitions on multilayer substrates, various transitions are designed for V-band and W-band applications as shown in Figure 5. Accurate alignment and compensating for fabrication errors are key challenges for fabricating high performance multilayer HDI transitions at these high frequencies. The ground vias are placed 20 µm from the edges and 400 µm apart as resonances are observed when the ground vias are placed 150 µm away from the edges. The via diameters are 50 µm, drilled with an excimer laser through a 2 mil LCP substrate ($\varepsilon_r \approx 3.05$ @ 60 GHz) with an accuracy of ±10 µm. The small via size minimizes the transition area and easily accesses any embedded circuits on the silicon wafer within the IC design rules avoiding large landing pads that degrade the overall performance. All of the dimensions are shown in Figure 6 and Table 2.

Figure 5 (a) shows a 1.6 mm long CPW line with vias connecting both parallel ground planes to the bottom ground plane. Figure 5 (b) shows a back-to-back vertical transition from one side to the other on a 2 mil LCP substrate. The via landing pads for the signal lines are 30 µm larger than the width of the lines to account for any misalignment. The gap between the ground plane and the area around the landing pad has been optimized to compensate for the parasitic inductance and capacitance from the via transition using Ansoft HFSS. A similar design of a CBCPW transition is shown in Figure 5 (c), but the bottom metal plane is embedded between the LCP and a silicon sample. The embedded bottom half is modified to maintain a good match to account for the effects by the placement of the silicon. Figure 5 (d) shows a back-to-back vertical

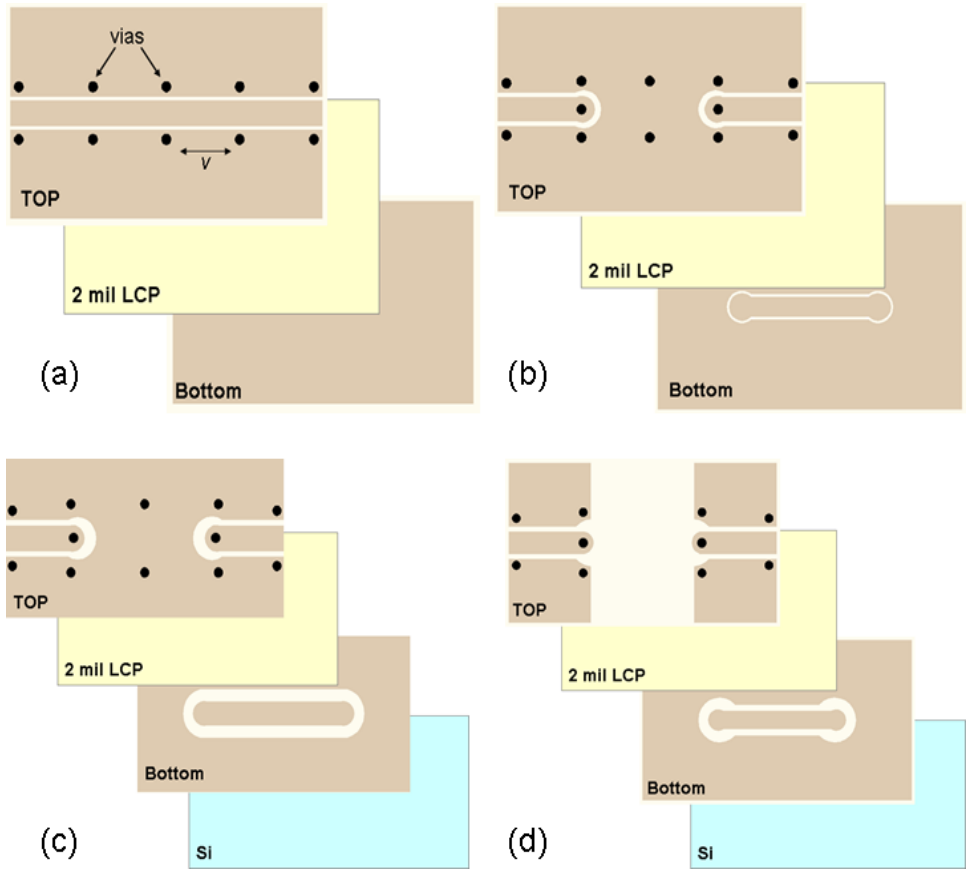



Figure 5: Layers of CBCPW transition designs (a) simple CBCPW line (b) CBCPW 3D transition on LCP (c) CBCPW 3D transition bonded to silicon (d) CBCPW to CPW 3D transition bonded to silicon.

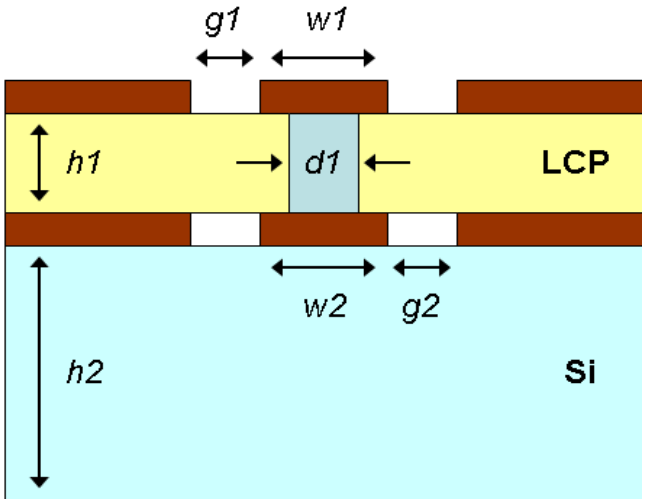



Figure 6: Side view of the multilayer stack up with its dimensions.

Table 2: Dimensions of Designs from Figure 6 (all units in µm)

| Fig. 1 | h1 | h2 | w1 | w2 | g1 | g2 | d1 |
|---|---|---|---|---|---|---|---|
| (a) | 51 | - | 105 | - | 40 | - | 50 |
| (b) | 51 | - | 105 | 80 | 40 | 20 | 50 |
| (c) | 51 | 525 | 105 | 100 | 40 | 90 | 50 |
| (d) | 51 | 525 | 105 | 80 | 40 | 60 | 50 |

CBCPW to CPW transition with optimized compensation around the signal via landing pads. The fabrication process starts with patterning the embedded layer, and then a 1 mil LCP bond ply, which melts at 285 $^{o}$C, is bonded in between a 1mil high melt LCP, which melts at 315 $^{o}$C, and a high-resistivity silicon for bonding. The vias are then drilled and filled with 4 µm of sputtered copper and then patterned. Although the edges inside the vias are thinner than the top metal, the skin depth above 60 GHz is less than 0.3 µm, and plating to fill the vias becomes unnecessary. The measurement is performed with an Agilent 8510C Vector Network Analyzer. Because of the complications of measuring

multilayer transitions, a back-to-back transition design is chosen and a Short Open Load Through (SOLT) calibration is performed for 150 µm pitch probes. Thus, the line loss is not calibrated out and a CBCPW line without a transition has been designed for comparison. The designs from Figure 5 (a) and 5 (b) are place on a hollow cardboard for measurements so that the bottom layer does not come into contact with the metal chuck. Figure 7 shows the measured results of a CBCPW line and the back-to-back vertical CBCPW transitions on LCP.

The CBCPW line exhibits more loss than expected as the estimated value is approximately 0.35 dB based on previous work [59]. The additional loss is partly attributed to the surface roughness of sputtered copper on LCP, which is about 1-2 µm and rougher than the copper clad material that was used in the previous work. Also, the vias are a source of radiation loss as they are placed closed to the edge where the E-field is highly concentrated. The overall loss of the vertical transitions and the lines is less than 2.1 dB with a return loss better than 17.1 dB in the entire band. The difference in the

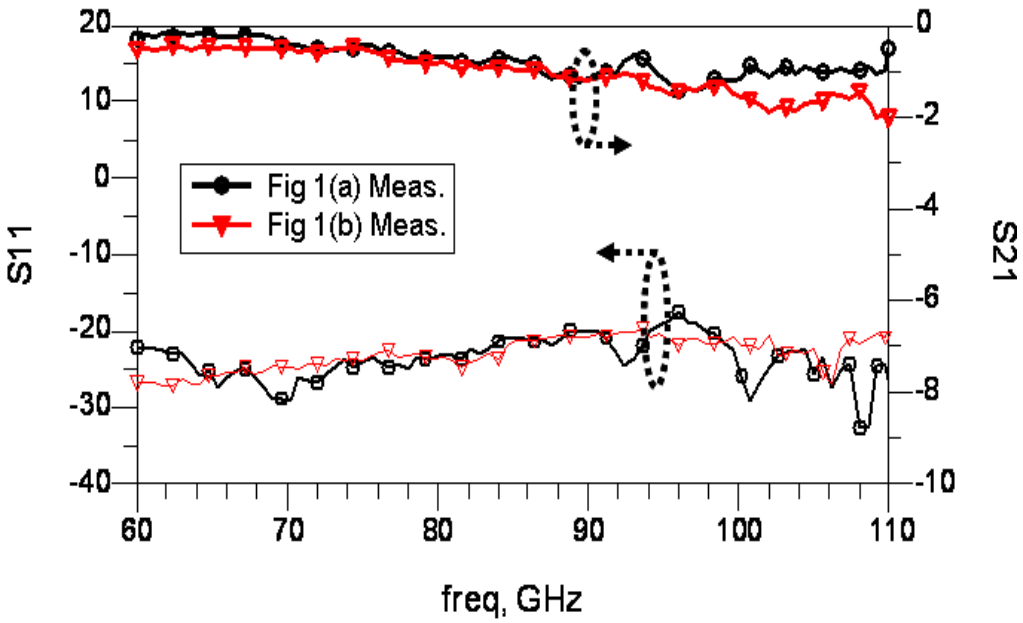



Figure 7: Measured results of a CBCPW line and a back-to-back vertical CBCPW transition on LCP, as shown in Figure 5 (a) and 5 (b).

overall loss is approximately 1 dB at 110 GHz, which translates to less than 0.5 dB per transition over the entire V-band and W-band. Figure 8 shows the measured response of the transitions on a single layer of LCP and LCP bonded to silicon at lower frequencies to verify the wideband performance. Both transitions show less than 0.1 dB of loss per transition up to 40 GHz compared to the CBCPW line that is used as a reference. Figure 9 shows the comparison of the simulated and measured performance of a back-to-back vertical CBCPW transition and a CBCPW to CPW transition for the LCP-Si case. The overall measured performance agrees well with the simulated values but it deviates as the frequency increases. This is due to the surface roughness becoming more of a problem at higher frequencies as well as the fabrication errors. The results of the CBCPW transition yield less than 2.2 dB of loss with a return loss better than 12.9 dB up to 100 GHz. Subtracting the measured line loss, the via transitions account for less than 0.5 dB per transition. The CBCPW to CPW transition shows an overall loss less than 1.7 dB up to 90 GHz and less than 3 dB up to 110 GHz and a return loss better than 14.1 dB up to 110 GHz. This translates to less than 1 dB of loss per transition up to 110 GHz.

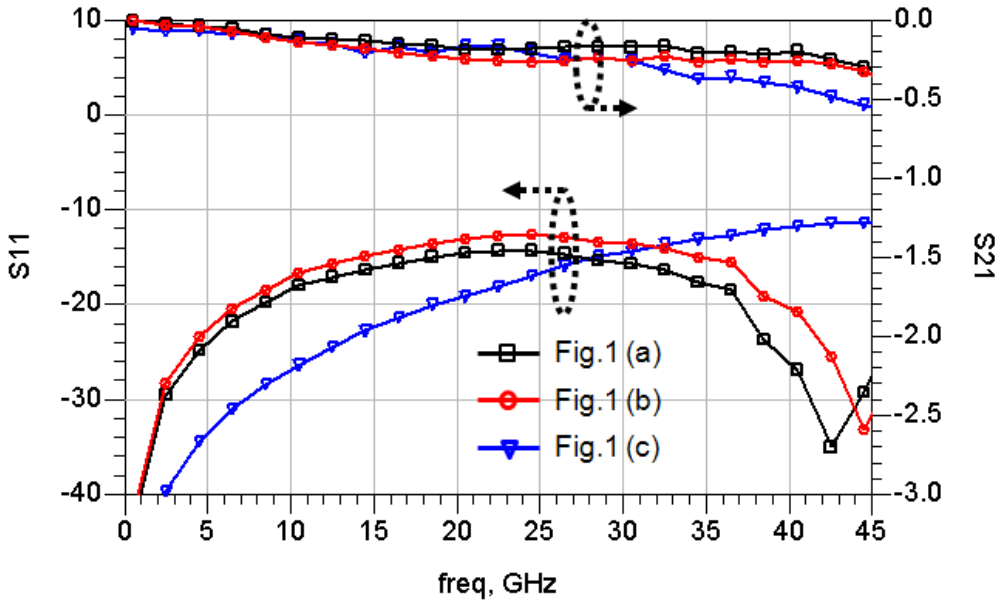



Figure 8: Back-to-back 3D via transition measurements up to 45 GHz.

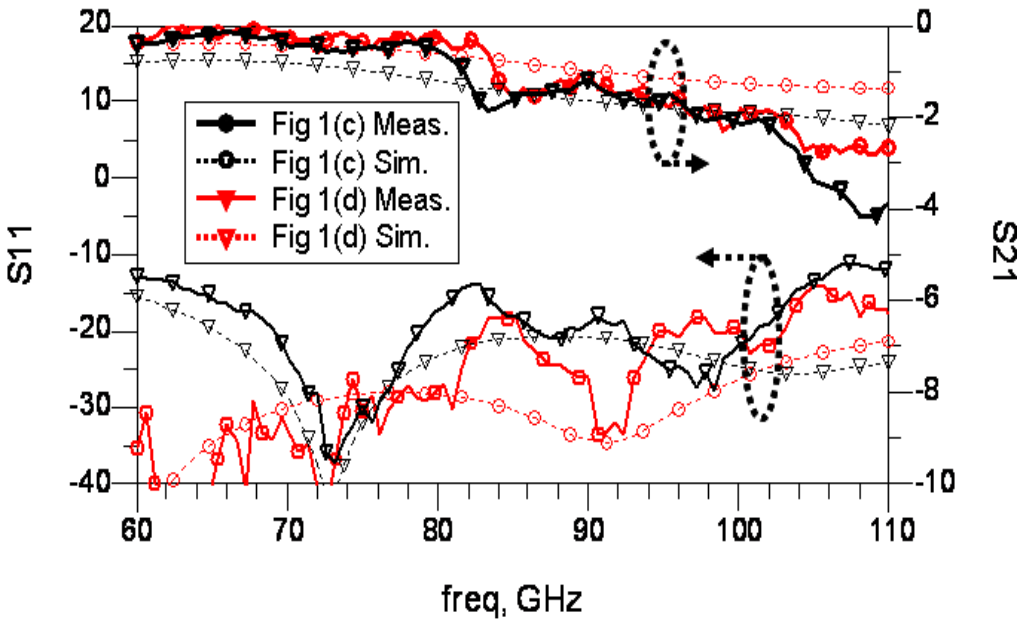



Figure 9: Simulated and measured results of back-to-back vertical transitions bonded to silicon, as shown in Figure 5(c) and 5(d).

Table 3 summarizes the extracted values for the equivalent model of a CPW via transition from Figure 2. The first two columns show the effect of the via size in a simulated comparison. The larger via has less parasitic effects. However, as the via becomes larger, the landing pad size grows in proportion that mainly contributes to additional parasitic capacitance. In addition, most IC chips have small input and output pads that are less than 80 µm x 80 µm. The extracted equivalent model values for the measured via are much larger than the simulated values. This is due to the fact that the vias are metalized using a sputtering tool, which results in a thin metal layer on the walls for the vias. The parasitic effects may be reduced by plating the vias thicker if needed.

Low loss and wideband performance via transitions have been designed, fabricated and measured on LCP as via technology is a crucial component for compact multilayer systems.

Table 3: Extracted values using equivalent model (Figure 2)

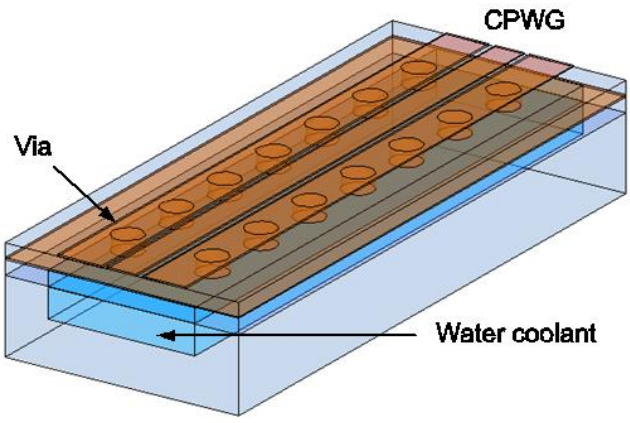
| | 50 µm via simulated | 80 µm via simulated | 50 µm via measured |
|---|---|---|---|
| $L_v$ | 49 pH | 40 pH | 64 pH |
| $R_v$ | 1.2 Ω | 1 Ω | 2.5 Ω |
| $C_t$ | 10 fF | 7 fF | 15 fF |
| $C_b$ | 20 fF | 14 fF | 29 fF |

## 2.3 Via Cooling

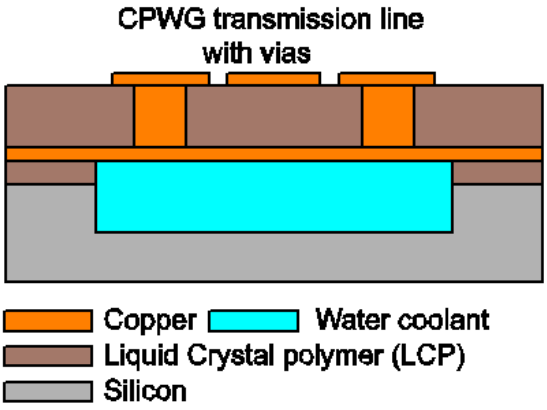
Thermal management in a RF system is crucial as the heat generated from the active components will quickly degrade the performance and eventually cause failure of the system. In a compact multilayer system, there is limited space for thermal management and removing the heat of embedded devices is a serious challenge. In addition, LCP has a low thermal conductivity of 0.2 W/m·K [19], making it difficult for the heat to dissipate through the substrate. Copper, on the other hand, is a good thermal conductor with a thermal conductivity of 401 W/m·K. Thus, it is essential to include metallic vias for effective thermal management of a multilayer LCP system.

There are three main approaches to removing heat from embedded devices. The first is to use thermal vias to connect to a heat sink [60], the second is to use heat pipes [61], and the third is to use microchannels carrying cooling fluids with an internal or external pump [62]. Each technique has its advantages and drawbacks, and in this chapter, the microchannel approach has been chosen because of the high power handling capability and efficient heat transfer. In addition, micropumps have become sufficiently powerful to cool complicated circuits without excessive power, volume, and weight demands [63].

A CPWG line is used to demonstrate an active via cooling technology. The schematic of this architecture is shown in Figure 10. The challenge of realizing this design is effectively laminating the LCP and Si to avoid leakage while maintaining a good contact filling the vias. The design and measurements is carried out at the Purdue University under Prof. Peroulis. The transmission line is 50 Ω with a 180 µm wide center signal line, 300 µm wide ground planes, and 30 µm gaps in between. The embedded ground plane is 100 µm below the CPW line and connected to the top layer ground planes with 200 µm diameter vias that are spaced 500 µm apart. The vias are used to increase the thermal conductivity between the CPW and the




(a)




(b)

Figure 10: Simple CPWG line for RF cooling system (a) 3D view (b) side view

microchannel that contains circulating water. The number and size of the vias dominate the interior thermal resistance of this architecture and the high thermal conductivity of the metallic vias offer low resistive traces for the heat to flow [63]. In addition to the thermal advantages, the small size of the vias allow great flexibility on their exact placement in an actual circuit. The embedded ground completely isolates the microchannel from the top RF lines. The dimension of the microchannel is 300 μm by 1 mm and carries water, which has a heat capacity of 4200 J/kg·K, as the coolant.

Figure 11 shows the simulated results of the temperature distribution of the CPW line with and without grounded vias using COMSOL multiphysics. A heat flux of 10 W/cm$^2$, which is relatively high for a RF circuit, is applied to the top CPW line while the bottom layer temperature is fixed to 25 $^{o}$C. The vias are assumed to be filled with silver epoxy that exhibits a high thermal conductivity of 3 W/m·K. The resulting temperature gradient of the line drops from 55 $^{o}$C (without vias) to 35 $^{o}$C with vias. The simulated

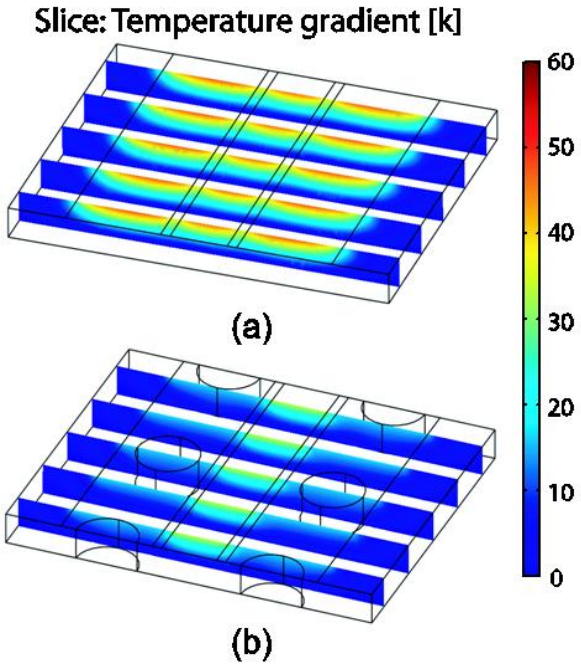



Figure 11: Simulated thermal gradient of CPWG lines (a) without vias (b) with vias.

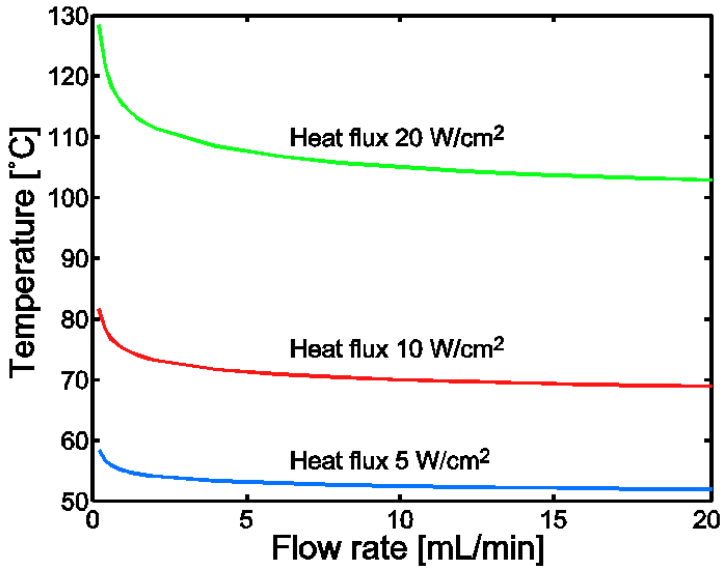



Figure 12: Simulated cooled-down temperature as a function of flow rate.

cooling efficiency of water is shown in Figure 12. The temperature of the input water is set to 35 $^{o}$C. The simulation results show that for a flow rate 10 mL/min, which is a reasonable rate for a mircropump [64], water cools the maximum temperature from 59/82/128 $^{o}$C down to 52/70/104 $^{o}$C when the heat flux is 5/10/20 W/cm$^2$ on a 1-mm long CPW.

The fabrication process is shown in Figure 13. Starting with copper clad on one side of the LCP, a $CO_2$ laser is used to drill 200 μm vias along with the input and output of the water channels. Then, 3 μm of copper is sputtered on the vias and filled with silver epoxy and the top layer CPW lines are patterned. Next, the microchannel is etched in a silicon substrate using $XeF_2$ gas. The third sample, which is LCP bond ply, is laser etched in the shape of the channel used to increase the channel height and also to bond the top layer to the silicon sample. After the laser etch, the residue is removed with $O_2$ plasma in a Reactive Ion Etch (RIE). Figure 14 shows $CO_2$ laser cut LCP before and after the samples have been plasma cleaned. Both samples have been cleaned with acetone in an ultrasonic bath but the residue is still present. Three minutes in the $O_2$ plasma removes

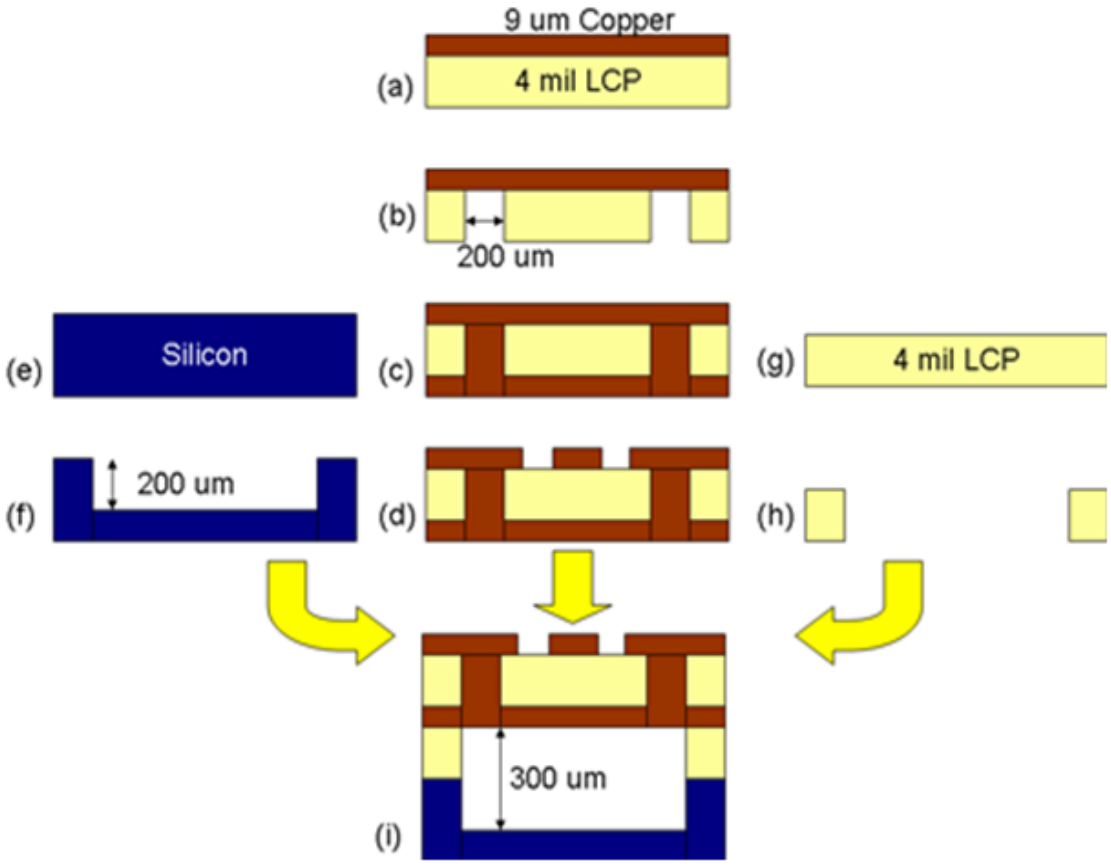



Figure 13. Process flow: (a) copper cladded LCP (b) $CO_2$ laser drilled vias (c) metalized vias (d) patterned CPW lines (e) 4 mil LCP (f) laser cut channels in LCP (g) bare silicon wafer (h) patterned channels (i) bonded final product.

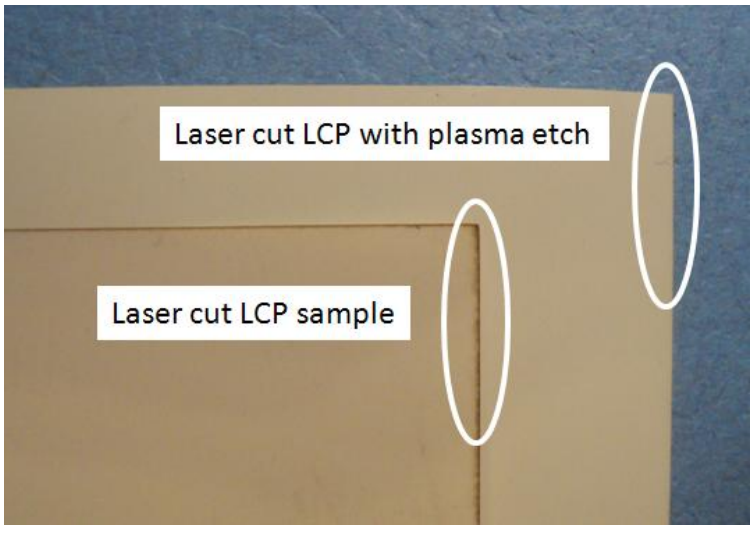



Figure 14: Comparison of $CO_2$ laser cut LCP before and after plasma cleaned LCP.

the residue completely. Once the three components are done, spray epoxy is used to bond the sample and it is cured at 120 $^{o}$C. Figure 15 shows the final sample with a micropump attached. The micropump size is 28 mm x 14 mm x 24 mm and operates with 6 V and 0.2 A. The measured response is compared to the simulated response with and without the water flow as shown in Figure 16. Since the ground plane is between the water channel and the top CPWG lines, the lines are completely isolated from the cooling water and the measured response is consistent with and without the water flow.

A successful hybrid integration of LCP and Si has been demonstrated to create an active cooling system using micro pumps. This shows the possibilities of thermal management of high power applications on a SOP platform with a low thermal conductor LCP.

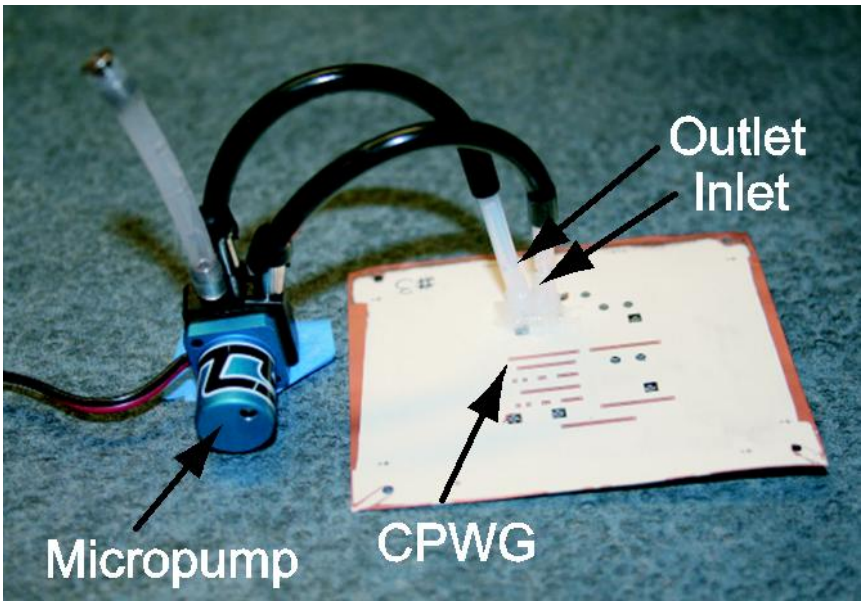
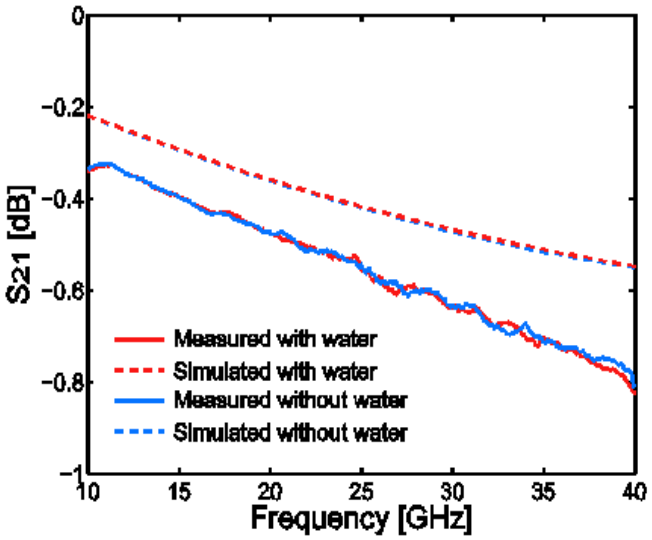
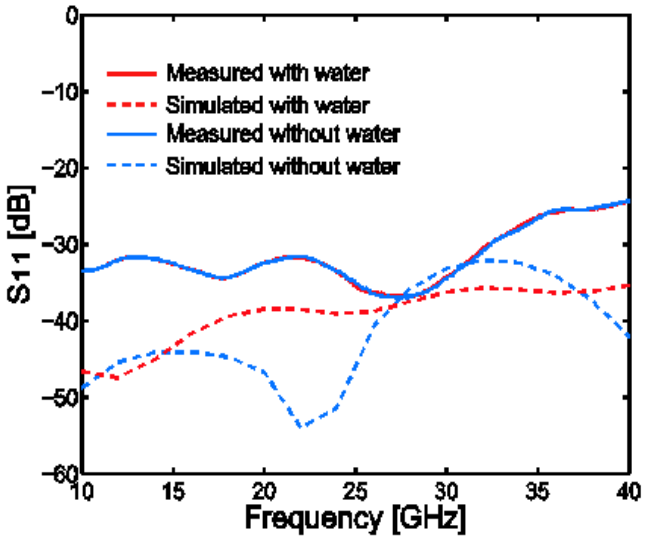



Figure 15: Completed active via cooling of a transmission line.




(a)




(b)

Figure 16: Measured and simulated results with and without water flow (a) $S_{21}$ (b) $S_{11}$.

## 2.4 Summary

In this chapter, via technology on LCP has been used to show HDI via transitions for low loss wideband applications and thermal vias for removal of the heat in embedded devices. This is the first time to demonstrate HDI via transitions on organic LCP and on

hybrid LCP laminated Si with frequencies up to 110 GHz. The thermal vias in LCP with the microchannels formed by LCP integrated with Si has been shown for the first time.

# CHAPTER 3

# RF MEMS ON LCP

RF MEMS switches have low loss, low power consumption, wideband performance, and high isolation. The ability to add reconfigurable attributes to a design helps create more powerful devices with multifunction. Though the switching time is slower than diodes at several microseconds on average, RF MEMS switches are suitable for specific applications, such as reconfigurable antennas, which can tolerate the switching speeds but require higher isolation. By integrating RF MEMS switches directly onto LCP, maximum compactness is achieved as extra bulky circuitry is avoided and the MEMS switches are designed to maintain the impedance in the design.

## 3.1 Background on RF MEMS Switches (Series Cantilever)

In this chapter, the most basic parameters of series cantilever type RF MEMS switches are studied. The pull-down voltage (electrostatic actuation), isolation, capacitive vs. ohmic switches, and switching speed are discussed.

### 3.1.1 Pull-down voltage

The pull-down voltage is the voltage at which the cantilever membrane has reached the two-third point in the gap for electrostaically actuated RF MEMS switch. At this point, the beam position becomes unstable due to positive feedback in the electrostatic actuation and the beam collapses to the bottom [26]. The cantilever beam is modeled as a mechanically small beam fixed on one end that has a spring constant k and mechanical stiffness $F_b$, where

$$k = 2Ew\left(\frac{t}{l}\right)^3 \frac{1-(x/l)}{3-4(x/l)^3+(x/l)^4}, \tag{2}$$

$$F_b = ky. \tag{3}$$

E is the Young's modulus, w is the width of the beam, t is the beam thickness, l is the length of the beam, and x is the starting position at which the force is distribute. The example is shown in Figure 17.

Meanwhile, the electrostatic force applied to the beam is a function of the time dependant capacitance and the applied voltage. The capacitance is a function of the gap, which is time dependant and changes with an applied force. The electrostatic force is given by the following [65],

$$F_e = -\frac{1}{2}\frac{dC(g)}{dg}V^2 = -\frac{1}{2}\frac{\varepsilon A V^2}{g^2}\ , \tag{4}$$

where ε is the effective permittivity, A is the area of the electrode, and V is the applied voltage. By equating equation (3) and (4) and solving for the voltage results in

$$V = \sqrt{\frac{2k}{\varepsilon A}g^2(g_o - g)}, \tag{5}$$

where $g_o$ is the zero voltage gap. Next, g is substituted by $(2/3)g_o$ to find the pull-down voltage,

$$V_{pd} = \sqrt{\frac{8k}{27\varepsilon A}g_o^3}\ . \tag{6}$$

Thus, to lower the pull-down voltage, the spring constant must be lowered by using

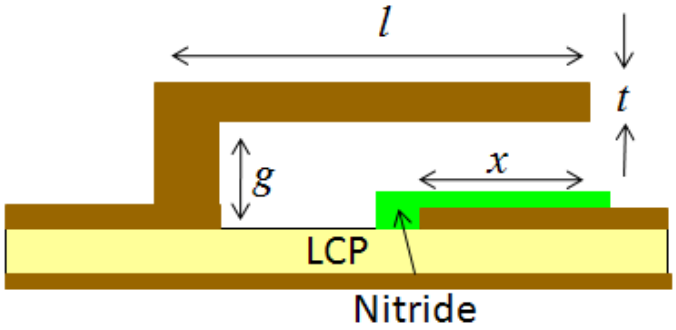



Figure 17: Cantilever type capacitive RF MEMS switch.

meanders and/or thinner lines. However, a lower spring constant sacrifices reliability of the switch and the switching speed. The pull-down voltage may also be lowered by reducing the gap but at the expense of reduced isolation discussed in the next chapter. Increasing the electrode surface area to apply more force also decreases the isolation. The designer must carefully study the tradeoffs and design for the best to meet his/her specifications.

### 3.1.2 Isolation

The equivalent electrical model of a RF MEMS switch at its up-state is a capacitor for both capacitive and ohmic switches. The isolation of a series switch is given by the following [66],

$$\left|S_{21}\right|^2 \approx 4\omega^2 C_{up}^2 Z_o^2 . \tag{7}$$

$\omega$ is the frequency, $C_{up}$ is the upstate capacitance, and $Z_o$ is the impedance of the transmission line. $C_{up}$ is a function of the gap and electrode area that applies the electrostatic force. Looking back to equation (6) of the pull-down voltage, it is clear that the isolation and the pull-down voltage have an inversely proportional relationship. Increasing the upstate capacitance for better isolation by increasing the gap and/or reducing the electrode area results in a higher pull-down voltage. The high voltage is problematic for integrated applications, where achieving more than 10 V requires extra circuitry and real estate for isolation.

### 3.1.3 Capacitive vs. Ohmic Switches

The switch shown in Figure 17 is a capacitive switch where as the switch in Figure 18 is an ohmic switch. Both are cantilever type series switches but the difference is in the contact surface. A capacitive switch has a thin layer of dielectric over the contact area to create an effective capacitor in the down state. Because of this down state

capacitance, the switch does not work near DC but rather above 10 GHz where the capacitor becomes an effective short. The insertion loss is given by the following equation [26],

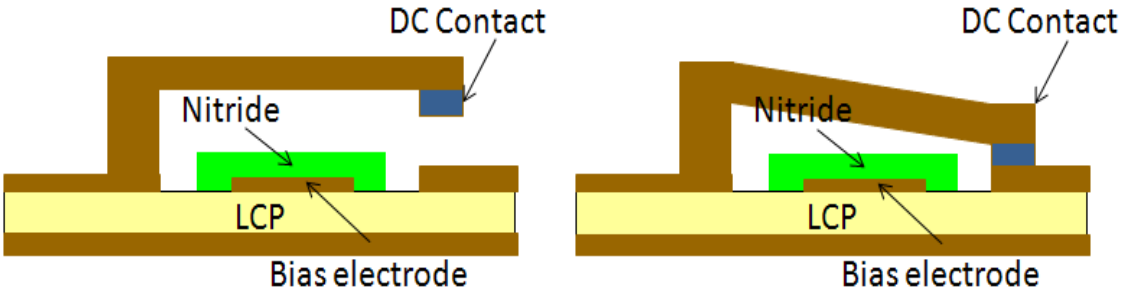
$$S_{21} = \frac{2jC_d Z_o}{1 + 2j\omega C_d Z_o}, \tag{8}$$

which is dominated by the down state capacitance. Ideally, the equation shows that with increasing frequency, the insertion loss improves. Since a larger area is used for contact, a capacitive switch allows more power handling than an ohmic switch. However, stiction is a problem where the membrane sticks to the dielectric. In addition, dielectric charging is another failure mechanism where charges are accumulated in the dielectric to shift the actuation profile and also cause stiction.

On the other hand, the ohmic switches make direct metal to metal contact at the surface. Because of this contact, the switch operates from DC but the switch inductance grows with the frequency to limit the operation around 60 GHz. The insertion loss of a direct contact switch is given by the following equation [66] for ($\omega L << R_s$)

$$S_{21} = 1 - \frac{R_s}{2Z_o}, \tag{9}$$

where $R_s$ is the contact resistance and L is the inductance of the switch. Since the contact resistance is in the order of 0.1 – 3 Ω depending on the metal and design, at low frequencies, the ohmic switches provide very low loss. The bias electrode as shown in




(a) (b)

Figure 18: Cantilever type ohmic RF MEMS switch (a) off state (b) on state.

Figure 18 (b) does not touch the membrane when actuated, and as a result, dielectric charging is not a problem. Since the contact is metal to metal, the contact area is minimized so that the membrane does not stick to the bottom contact. At higher frequencies above 40 GHz, the loss is dominated by the inductance of the switch limiting the performance of the device. The contact force is in the order of tens of μN to a couple mN. Though a higher contact force is desired for less resistance, the higher force wears the contact faster, which is the main cause for switch failure.

### 3.1.4 Switching time

The switching time of RF MEMS switches is in the order of microseconds, which is slow in comparison to PIN diodes or FET switches that operated in the nanosecond range. The actuation is mechanical rather than electrical, which limits the switching time. The release time however, is dependent on the restoring force of the spring constant that is less than the force from the actuation voltage. Therefore, the release time is greater than the switch time. The mechanical motion of the cantilever is simply described by the steady-state solution for a driven oscillator as follows [67],

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx = F_{ext}, \tag{10}$$

where m is the mass, b is the damping coefficient, k is the spring constant, $F_{ext}$ is the exerted force, and x is the displacement. The closed-form solution for a beam with small damping coefficient ($b \approx 0$) and a quality factor $Q \geq 2$ [22] is obtained by substituting in equation (4),

$$t_s = 3.67\frac{V_{pd}}{V_s\omega_o}, \tag{11}$$

where

$$\omega_o = \sqrt{\frac{k}{m}}, \tag{12}$$

which is the resonant frequency.

Figure 19 shows the layout of the switch under test for measuring the switch speed. The switch dimensions are 330 µm by 252 µm. The 252 µm is the width of a 50 Ω line on 4 mil LCP. The bias voltage is given directly on the line with the RF signal where one side of the switch is the positive voltage and the other side is grounded. The middle section is etched away to create two 28 µm beams supporting the membrane to lower the overall spring constant for lower actuation voltage. As a result, the pull down voltage is only 10 V.

Figure 20 shows the block diagram of the setup used for switch measurement. The function generator is used to generate a square waveform to turn the MEMS switch on and off at 1 kHz. The bias tees are used to protect the equipment from the DC bias. A crystal detector is used to detect the variation in voltage of the MEMS switch, which is in the order of tens of mV. This variation in voltage corresponds to the on-off actuation of the MEMS switch. The MEMS switch is equivalent to a variable capacitor and the variation in voltage is from the voltage across the MEMS switch. The output of the crystal detector is read in the oscilloscope along with the function generator output. The switching time and release time are defined to be the time it takes to reach 90 % of the

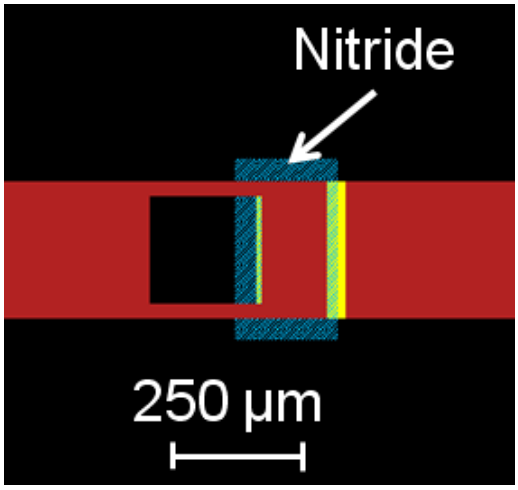



Figure 19: RF MEMS switch layout used to measure the switching speed.

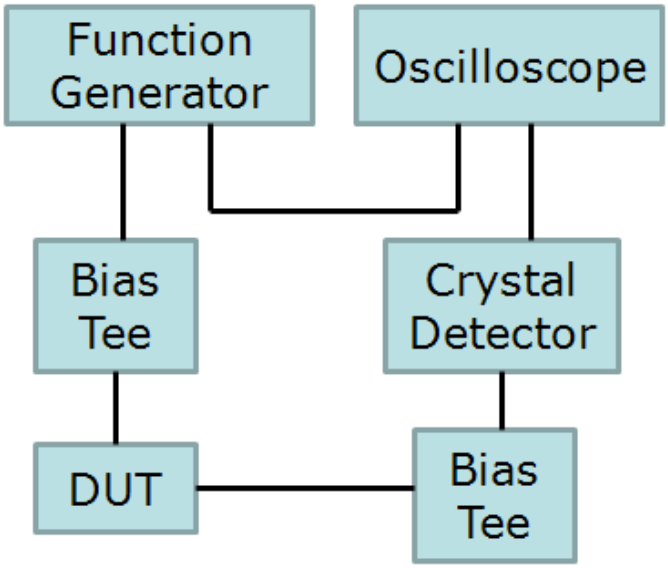



Figure 20: Block diagram of MEMS switching time measurement setup.

total variation in voltage. Figure 21 shows the actual setup of the MEMS switching time measurement. The Device Under Test (DUT) is on a probe station that is not shown in the picture. Table 4 shows the measured switching time, release time, and the calculated time using equation (11) according to the actuation voltage. Figure 22 shows the plotted data. The switching and releasing time is very slow at the pull down voltage and increases rapidly with the higher actuation voltage. The discrepancies in the lower and higher end of the graph come from the limitations in equation (11) as assumptions are made for simplification purposes. The release time is naturally slower than the switching time as the release of the switch depends on the mechanical restoring force of the cantilever membrane. Researchers are continually working on lowering the switching speed into the nanosecond range closer to that of diodes and FET switches.

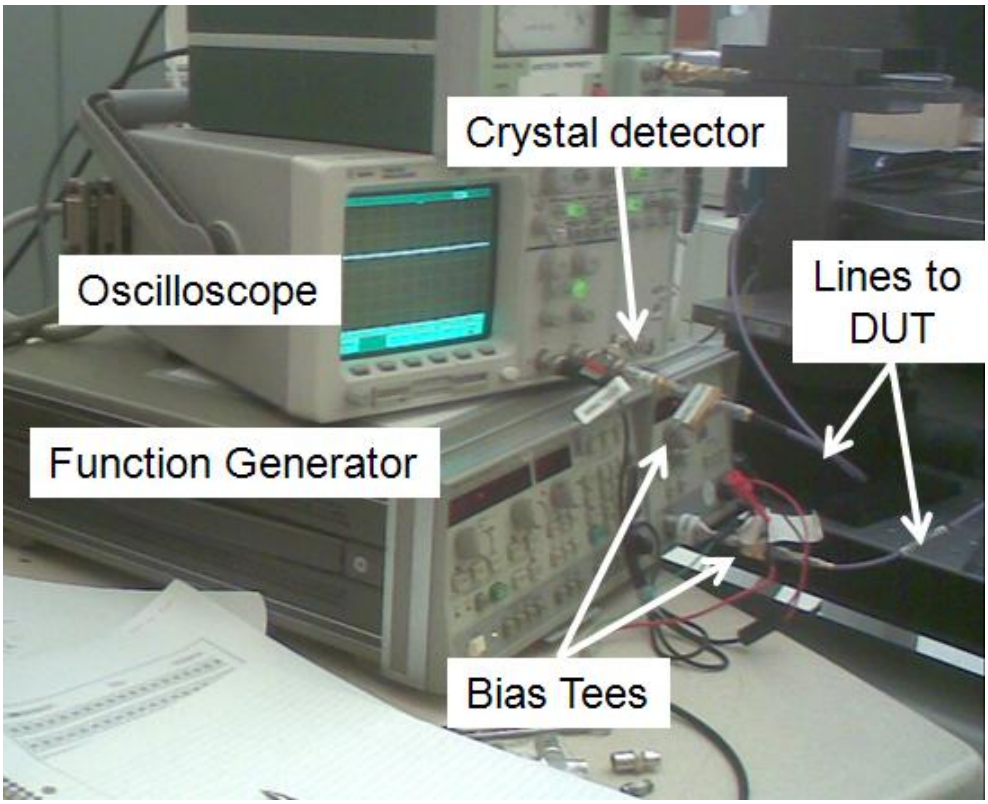



Figure 21: Picture of MEMS switching time measurement setup.

Table 4: Measured and calculated switching time and release time of the cantilever switch shown in Figure 18.

| Applied Voltage (V) | Switching Time (µs) | Calculated Switch Time (µs) | Releasing Time (µs) |
|---|---|---|---|
| 10 | 224 | 118.8 | 480 |
| 15 | 97 | 79.22 | 102 |
| 20 | 62 | 59.41 | 84 |
| 25 | 11.8 | 47.53 | 69 |

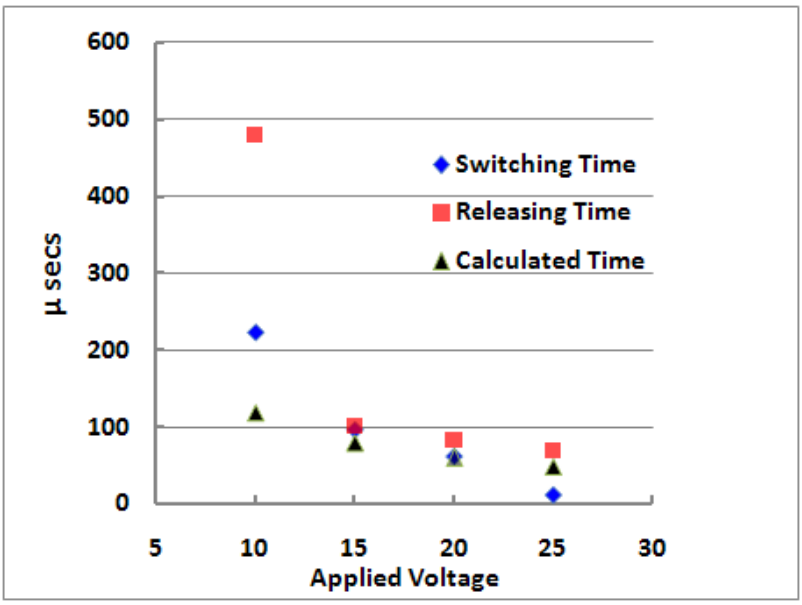



Figure 22: Table 4 plotted.

## 3.2 Fabrication of RF MEMS Switch on LCP

Fabrication of RF MEMS switches directly on LCP is not conventional and only a handful of researchers have successfully published their work. Only a couple additional steps are required compared to typical RF MEMS switch fabrication on standard substrates such as Si or quartz. However, caution is required in every fabrication step as misalignment and warping of the substrate are fatal to the process. The first process for RF MEMS switch fabrication on LCP was developed by Dr. Guoan Wang and Dr. Nicholas Kingsley and the details of the process flow are well documented [68], [69]. In this chapter, minor revisions to the original recipe are included as well as the author's comments on each step.

The material that is used is Rogers Ultralam 3850. First, the copper clad from the LCP material needs to be etched off using nitric acid. LCP without copper clad is provided but the copper clad material goes through a nitrogen treatment that works better with the deposition processes to follow. The subsequent steps are dependent on the design. For multilayer designs, the embedded layers are patterned and the stack up is

bonded before polishing since the heat and pressure of the bonder roughens the surface. Laser drilled alignment holes and vias are also created before polishing since the plasma cleaning of the residue roughens the LCP surface as well. Once these steps have been finished the surface of the LCP must be polished as the initial surface roughness is around 1 μm. The polished LCP has a surface roughness less than 50 nm. A Lapmaster polisher has been used that allows up to three 4 inch wafers to be polished under 30 mins. When polishing thin and small pieces of LCP, the samples tend to kick out of the weights as not enough surface area is available for holding the sample. It is best to have a larger sample for polishing and to round any sharp edges for better polishing. In addition, reducing the pressure and gradually increasing the rotation speed over a few minutes may help solve this problem. If the sample is still not holding up, a slower rate may be applied for a longer time. Ideally, the sample is polished at 55 rpm for 25 mins under 16 lbs of weight. The polishing speed and quality are a function of the rotation speed, time, and pressure.

Once the sample is polished, the surface needs to be cleaned with acetone, methanol, and Isopropyl Alcohol (IPA). To clean the surface thoroughly, a wet cotton swab may be used to gently and very lightly scrub the surface without scratching the LCP. Next, a thin layer of Ti/Au (200 Å/ 2200 Å) is deposited at a rate of 3 Å/s for the Ti and 2 Å/s for the Au on the polished surface using e-beam, or electron beam, deposition. This layer is the seed layer used to define the bias for actuating the MEMS switch. For the e-beam deposition, a better quality metal film is obtained by lowering the pressure at the time of deposition. With a lower pressure, fewer particles are present in the chamber and the mean free path of the metal particles increases to yield a more uniform deposition [70]. Typically, the vacuum pressure should be under $2 \times 10^{-6}$ Torr. The thin Ti layer helps in the adhesion of the Au layer. The Ti layer thickness has been varied from 125 – 250 Å and no noticeable difference has been observed. However, the e-beam machine has its limitations to its deposition accuracy. Both too thin and too thick of a Ti layer cause

de-lamination of the metal in the sequential steps. Au is used for the metallization because it has a high conductivity and does not oxidize. The deposited metal is patterned using standard lithography. Shipley 1827 photo resist is used with a thickness of approximately 1.8 µm, which is achieved by spinning at 500 rpm for 5 secs and 3000 rpm for 30 secs. The thickness varies with the spin and with different surfaces and 3000 rpm on LCP yields a photo resist thickness of 1.7 – 2.0 µm. It is essential to use clean photo resist and eliminate all bubbles in the photo resist before spinning. In addition, before every step, it is best to blow the sample off with a nitrogen gun to ensure no particles are sitting on the sample. The baking and exposure time are stated in the chemical data sheet [71]. Positive photo resist is forgiving in over baking and over exposing. It is better to over bake or over expose as if it is under baked, the photo resist will stick to the mask and peel off the photoresist. If it is under expose, the sample will not develop and etch properly. Another option is to use Shipley 1813, which is a diluted version of 1827. At 3000 rpm, the thickness on LCP is 1.2 – 1.4 µm. The thinner thickness is also commonly used for the sacrificial layer of a MEMS process. The thickness of the photo resist may be varied by diluting the photo resist with a solvent of the same type. Shipley 1813, 1827, and SPR-220 use Propylene Glycol Monomethyl Ether Acetate (PGMEA) as its solvent. Once the photo resist is developed in Microposit MF -319 developer for approximately 2 mins or until no more photo resist is being removed, the metal is etched with Au etchant and Ti etchant. The Au etchant used is Transene GE/-8148 that etches at 50 Å/s [72]. The etch rate decreases as the solution is reused multiple times, which is beneficial in a sense that the features will not be over etched when defining fine features less than 50 µm. The Ti etchant is Hydrofluoric (HF) acid diluted 1:10 or 1:20 with De-ionized (DI) water that etches the deposited Ti within 15 secs. After the metal is etched, the patterned photo resist is removed with acetone and rinsed with DI water. If the acetone is not rinsed immediately photo resist residue that is hard to remove will remain and cause problems in the subsequent steps. This must be removed by a descum recipe that uses $O_2$ plasma in

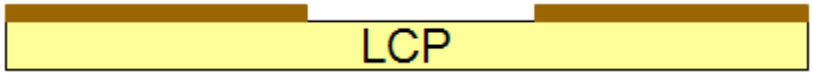



Figure 23: Seed layer patterned on polished LCP.

the plasma thermal RIE. An alternative would be to flood expose and develop the remaining photo resist. Yet another option would be to use photo resist stripper. A side view of the result or the first layer deposition and patterning is shown in Figure 23.

The seed layer is followed by a 2000 Å silicon nitride layer. This layer protectively coats the bias electrode for ohmic MEMS switches or creates the dielectric layer for capacitive MEMS switches. A Unaxis Plasma-Enhanced Chemical Vapor Deposition (PECVD) is used to deposit at 150 $^{o}$C. The standard deposition is at 300 $^{o}$C but the LCP bond ply material melts at a temperature of 285 $^{o}$C. Thus, the deposition temperature is lowered and this allows for deposition of a lower stress film at the cost of the nitride quality. As this step may be the place where the sample is exposed to the highest temperature, it is important to lay the sample flat with glass slides. In fact, at every baking step, the LCP sample must be placed as flat as possible and preferably have the edges pressurized. LCP films that are under 8 mils tend to curl while thicker films tend to stay manageably flat. However, with an exposure to 150 $^{o}$C, there is a tendency for LCP to shrink. It is advised to have the MEMS switches closer to the middle within a 2 inch square for alignment accuracy of 10 µm. A possible solution under investigation is to pre-bake the sample before the first layer deposition. The finished deposition should have a pinkish color on top of the gold. The thicker the silicon nitride film is, it will turn to yellow (~ 2200 Å) and then to a bluish reflection (~ 2500 Å). Once the silicon nitride is deposited, standard lithography is used to pattern the silicon nitride resulting as shown in Figure 24. The plasma thermal RIE tool may be used for a dry etch or diluted (HF:DI = 1:10) HF acid may be used to wet etch the silicon nitride film. When using the RIE, the chamber needs to be clean or otherwise, particles back deposit onto the substrate. Again,

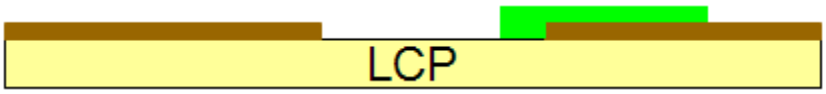



Figure 24: Nitride layer deposited and patterned.

the photo resist is moved using acetone once the etching is done.

At this point the backside, which is the ground plane, may be deposited with Cu if needed using a DC sputterer and patterned as shown in Figure 25. Cu is chosen as the metal for the back plane because it is affordable to deposit a thick layer and it has the second best conductivity out of commonly used metals after silver. Depending on the frequency, a thickness of 3 – 5 μm may be deposited. Considering the skin effect, where the amplitude of a current on a conductor reduces by 1/e for every skin depth travelled in the z-direction, four to five skin depths is a good thickness for the conductors. The skin depth is defined by the following equation:

$$\delta_s = \sqrt{\frac{2}{\omega\mu\sigma}}, \tag{13}$$

where ω is the frequency is radians, μ is the permeability, and σ is the conductivity of the metal. The back plane must be sputtered before the sacrificial layer as the sputtering process is hot enough to boil the photo resist. It is important to protect the top surface so that it is not scratched in the process. A layer of photo resist easily does the job.

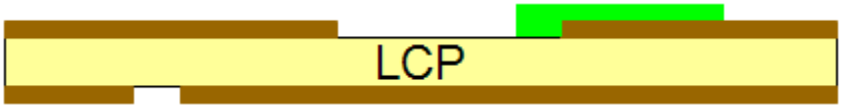



Figure 25: Back plane Cu sputtered and patterned.

Next, the sacrificial layer is patterned with photoresist, either 1827 or 1813 as shown in Figure 26. The thickness of the photo resist determines the membrane height, which is a tradeoff of isolation of the switch on the off state and the pull-down voltage as

mentioned in the previous chapter. After the developing step, the patterned photo resist must be hard baked so that in the subsequent step, it will boil up. The hard bake is done at 145 $^{o}$C for 8 mins in the oven. If the photoresist is not baked long enough, the photoresist will boil up while depositing the bridge layer, in which the sample is ruined at that point. If the photoresist is over baked, the photoresist will not be removed in the release stage and the RF MEMS switch will not actuate. Once the hard bake is finished, acetone should not be used in any of the following steps unless using it to release the membrane.

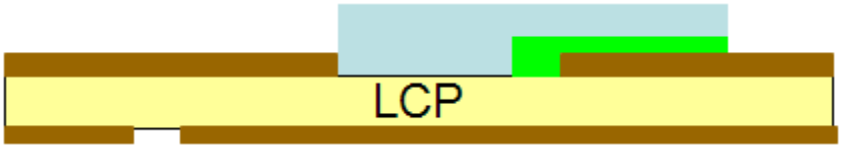



Figure 26: Sacrificial layer spin coated and patterned.

The e-beam evaporator is used to deposit the Ti/Au/Ti (200 Å/ 2200 Å / 200 Å) bridge layer, which is used to define the pattern for electroplating. The rate of deposition needs to be lowered (Ti: 2 Å/s, Au: 1.3 Å/s) to ensure that the chamber does not become too hot. Next, 1827 or SPR-220 is spin coated on the sample. 1827 is used for a final thickness under 2.5 µm and SPR-220 is used for thicker membranes up to 8 µm. Since the sacrificial layer is under the metal, a lower temperature of 80 $^{o}$C is used to bake the photo resist. A dark mask, or reverse polarity mask, is used for patterning this layer. Once the photoresist is exposed and developed, the sample is dipped into Ti etchant to pattern just the top Ti layer. A small area at the edge should also be exposed and etched for the electroplating clip. The top Ti layer is an extra protective layer under the photoresist for the electroplating. In addition, the photoresist may be hard baked under 100 $^{o}$C to ensure that the electroplated gold does not grow outside the pattern.

Before electroplating the membrane, it is important to make sure that the surface is clean. Also, a profilometer is used to measure the thickness of the patterned photoresist

to keep track of the thickness of the plated Au. The cyanide solution used for gold electroplating is heated to 55 $^{o}$C and stirred around 150 rpm with a magnetic rod while making sure a vortex is not formed in the solution. The current is set to have a current density of approximately 10 mA/cm$^2$. This gives a rate of 0.5 – 0.7 µm/hr. If the rate is too fast, the quality of the metal reduces and may peel off. In addition, air bubbles should not be present on the surface of the sample, which impedes the growth of Au. After 10 mins of electroplating, it is recommended to re-measure the thickness of the photoresist to check the deposition rate and adjust the current accordingly. Initially, the MEMS membranes have been plated to 2 – 2.5 µm. However, at this thickness, the membranes have a slight curl upward that increases the pull-down voltage and in some cases, the switch does not actuate at 110 V. Therefore, a membrane thickness of 3 – 5 µm is recommended when using gold membranes. Once the electroplating is finished, the sample is flood exposed and developed to remove all photoresist. The sample is dipped in Ti etchant, then Au etchant, and finally back into Ti etchant to remove all the metal that has not been plated. The resulting sample is shown in Figure 27. The sample is then placed in 1165 photoresist stripper for 10 – 16 hrs at 50 $^{o}$C. 1112 photoresist stripper is recommended for substrates other than LCP.

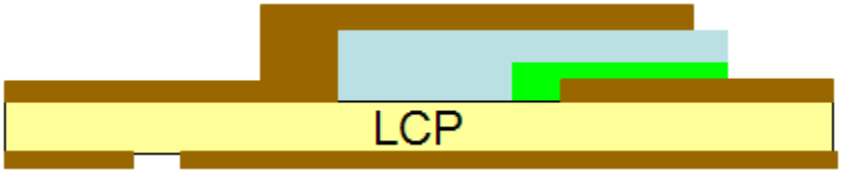



Figure 27: Bridge layer electroplated and patterned.

To remove the 1165 solution completely out underneath the membrane, the sample is placed in DI water for 5 mins and then IPA for 5 mins. This sequence is repeated three times. The sample is dried using a $CO_2$ critical point dryer. The side view of the finished sample is illustrated in Figure 28. The top view of the fabricated

capacitive RF MEMS switch is shown in Figure 29 that has a measured actuation voltage of 80 V.

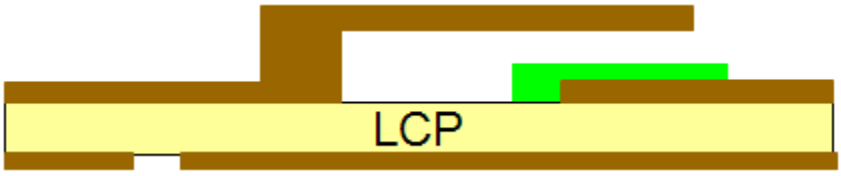



Figure 28: Released MEMS switch.

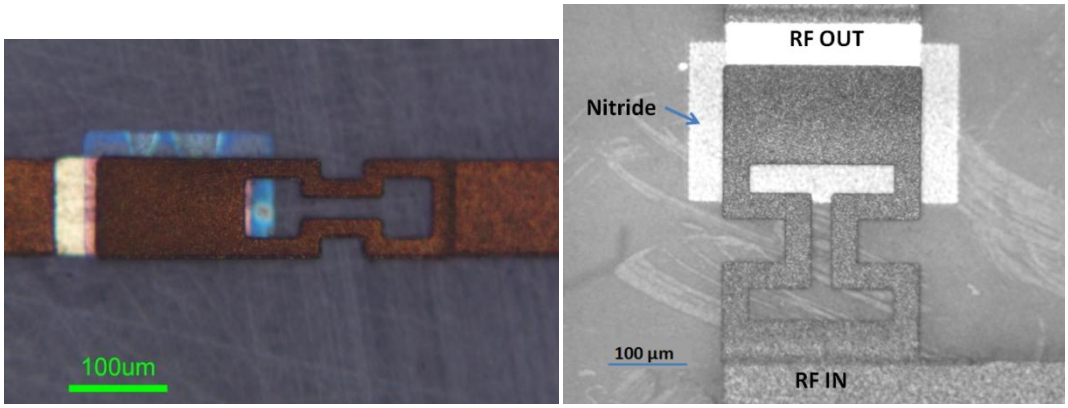



Figure 29: Fabricated capacitive RF MEMS switch.

## 3.3 Reconfigurable Antenna on LCP

Using the capacitive MEMS described in the Chapter 3.2, a compact pattern reconfigurable antenna is designed for MIMO applications. It has been shown that pattern reconfigurable antennas in a 2 x 2 MIMO system significantly improves the capacity compared to a fixed antenna [73]. The monolithically integrated RF MEMS switches allow a compact antenna design that would have otherwise not been realizable. Integrating an active IC chip or a RF MEMS chip takes too much real estate as it requires a large and complicated biasing circuitry. In addition, all additional components and metal traces interfere with the antenna radiation patterns. Therefore, monolithically

integrated RF MEMS switches that require minimal additional area are necessary for compact reconfigurable antennas.

The pattern reconfigurable antenna design is shown in Figure 30. The design of the antenna was done at University of Illinois at Urbana Champaign under professor Bernhard. The antenna is a microstrip structure that provides either broadside or endfire radiation pattern characteristics over a shared impedance bandwidth. Switching between the patterns is accomplished by changing the states of two integrated RF MEMS switches. Figure 31 shows a block diagram of the operation of the two modes. The biggest challenge is the design of the antenna within the constraints set by the fabrication process. The design requires one via to ground and another via that enables probe feeding of the antenna from the backplane. The design constraints come from the fact that the shapes and dimensions of the vias affect the antenna's impedance and radiation behavior so that the design must carefully take into account the fabrication tolerances. Figure 32 shows nine fabricated reconfigurable antennas on LCP. The individual size of the

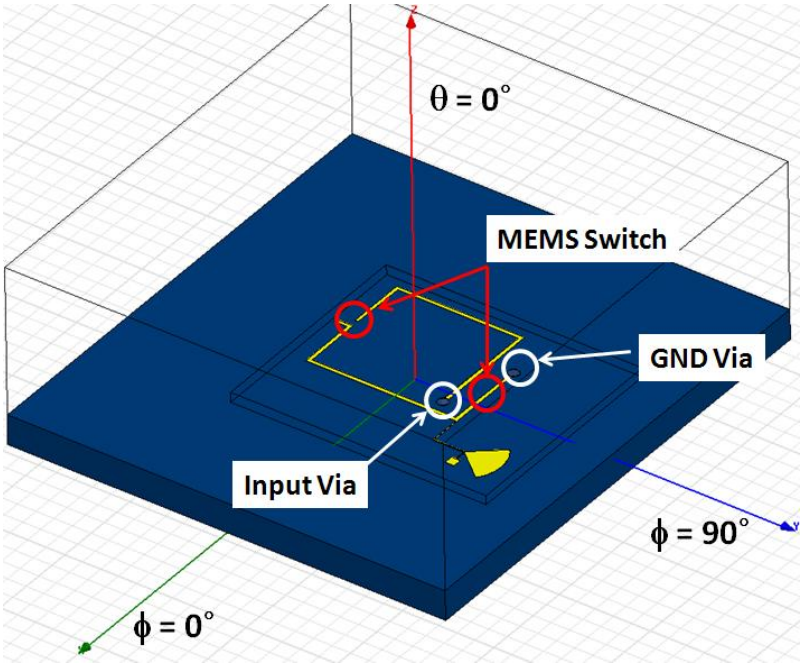
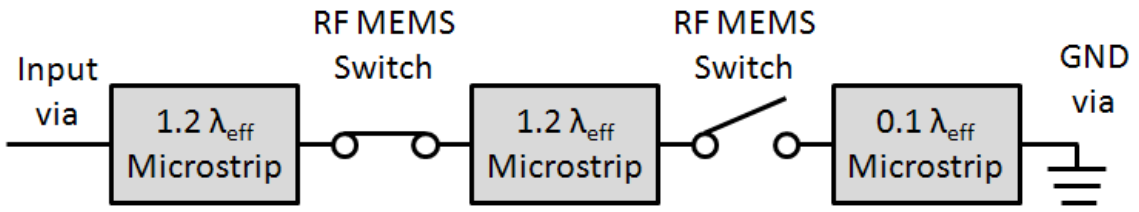
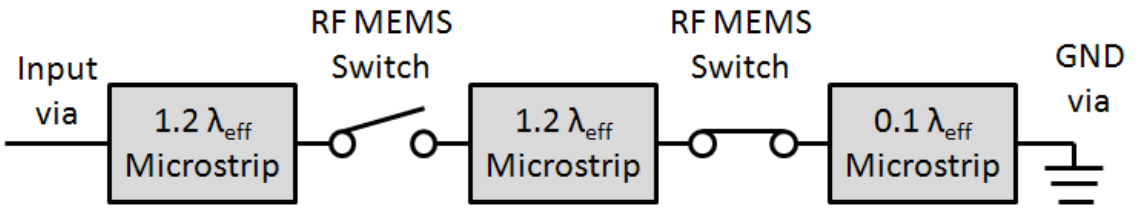



Figure 30: 3D model of pattern reconfigurable microstrip spiral antenna.




(a)




(b)

Figure 31: Block diagram of (a) endfire mode (single turn spiral antenna) (b) broadside mode (microstrip patch type antenna)

antenna is 3.5 mm by 4 mm and approximately 6 mm by 7 mm including the bias line. The bias line is designed as a quarter wavelength line with a radial stub that is equivalent to an additional quarter wavelength. The bias pad is connected to the point where the bias line and stub meet. From the tip of the radial stub that is open circuit, the RF signal travels a quarter wavelength to create a short circuit where the bias pad is connected so that no RF will leak. Again, from that point, the RF signal travels another quarter wavelength to become an effective open circuit looking from the antenna signal line. The operating frequency is 30 GHz, which enables a relatively thin substrate (0.8 mm) to provide the necessary impedance bandwidth for reconfiguration. The operation of the antenna is described in detail in [74], [75]. The feed is inputted from the back plane with a coaxial line through the input via. The endfire mode is achieved with the switch on the left closed and the switch on the right open respectively from Figure 30,which creates a single loop spiral antenna. The broadside mode is achieved by turning the left switch off

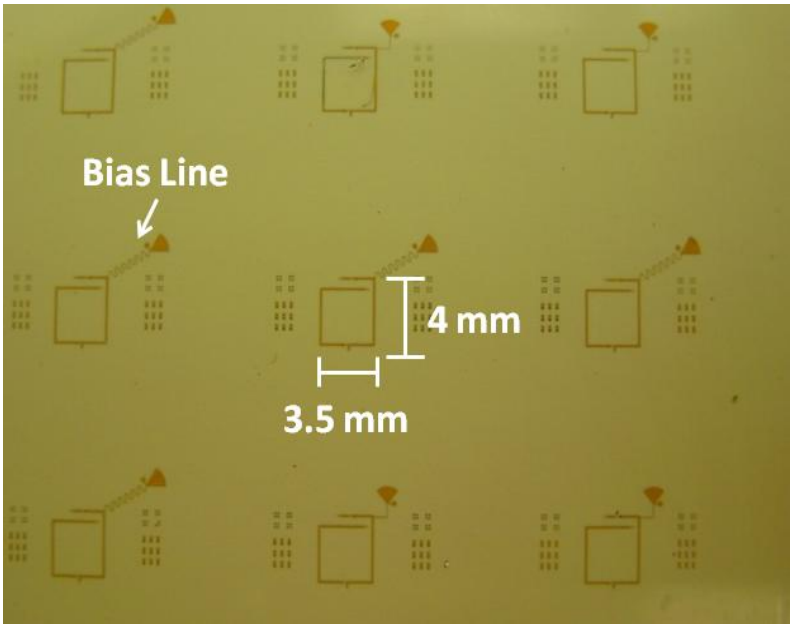



Figure 32: Nine fabricated reconfigurable antennas on LCP.

and the right switch on to create a cavity type antenna.

The antenna design is simulated and optimized using Ansoft HFSS. The simulated $S_{11}$ results shown in Figure 33 show that the broadside mode has a center frequency of 29.6 GHz with $S_{11}$ equal to -14.54 dB while the endfire mode has a center frequency of 29.3 GHz and $S_{11}$ of -11.92 dB. The bandwidth of broadside mode is 617 MHz or 2 % fractional bandwidth while the endfire mode has a bandwidth of 340 MHz or 1.13 % fractional bandwidth with a common impedance bandwidth of 207 MHz. Figure 34 provides the radiation pattern simulations for the broadside mode with a ground plane size of 1.3 $\lambda$ by 1.2 $\lambda$. The simulated radiation patterns for the endfire mode with the same sized ground plane are provided in Figure 35. The main plane of reconfigurability for this design is the $\phi = 0°$ plane while the main polarization of reconfigurability is $E_\theta$. A clear change in the radiation pattern is observed from the broadside mode to an endfire mode.

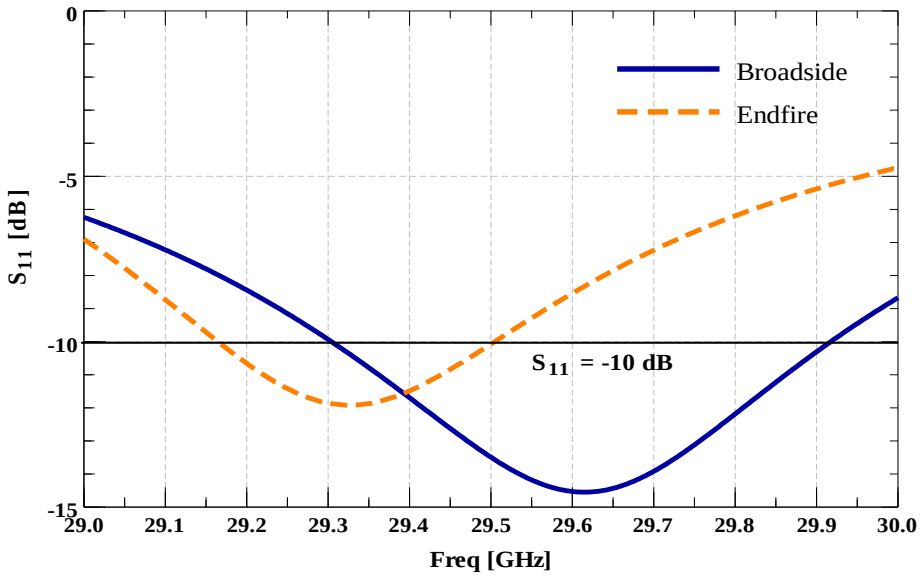
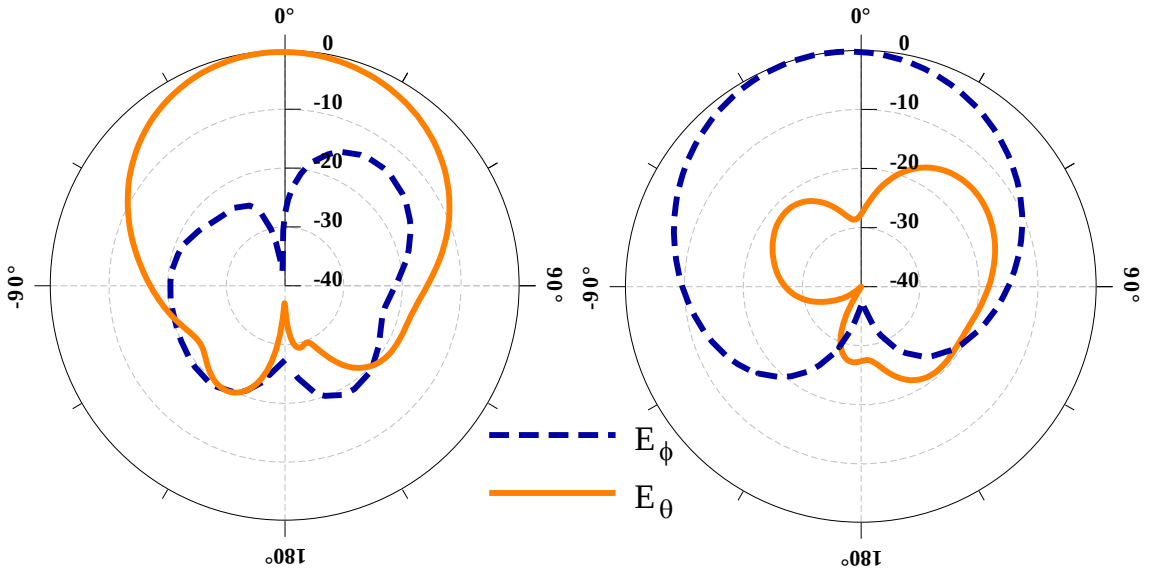



Figure 33: Simulated $S_{11}$ results of the reconfigurable antenna.

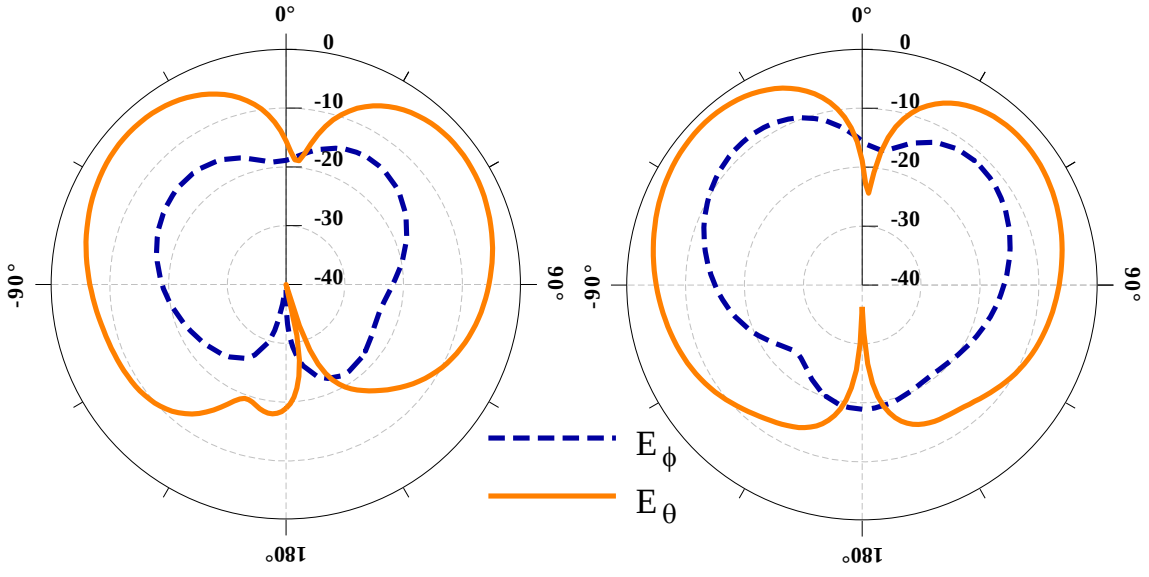
The measured $S_{11}$ broadside mode shows an operational frequency of 29.25 GHz with a match of -11.49 dB and the endfire mode is centered at 29.24 GHz with a match of -10.46 dB. Measured radiation patterns for the broadside and endfire modes are shown in Figure 36 and 37, respectively. Figure 36 exhibits a characteristic broadside pattern with most of the power radiating in the $\theta \approx 0°$ direction. The endfire mode shown in Figure 37 radiates off-center with maximum power radiated at $\theta \approx 60°$ and $\theta \approx -60°$ and depressions at $\theta \approx 0°$. The discrepancies in the simulation and the measurements can be attributed to several factors, such as ideal simulation, fabrication errors, and measurement noise.

RF capacitive MEMS switches have been successfully integrated on LCP to create a pattern reconfigurable antenna. By monolithically integrating the switches directly on LCP, the small antenna is realizable with minimal distortion to the antenna pattern. An RF ohmic MEMS switch that is monolithically integrated to create another reconfigurable antenna is shown in Appendix A.



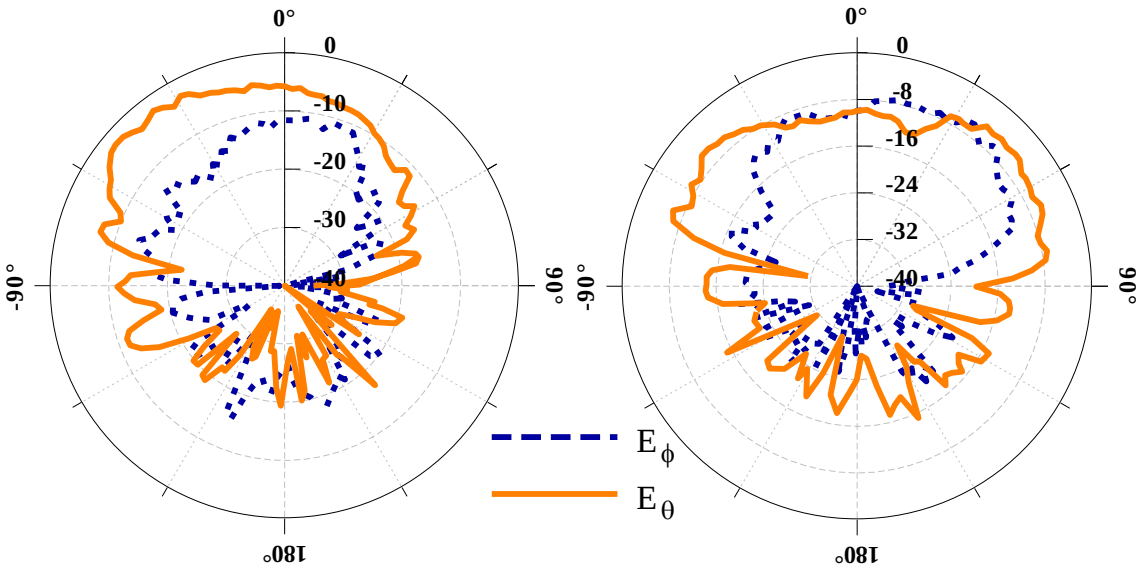

(a) (b)

Figure 34: Simulated radiation patterns for broadside mode for (a) ϕ = 0° and (b) ϕ = 90°.



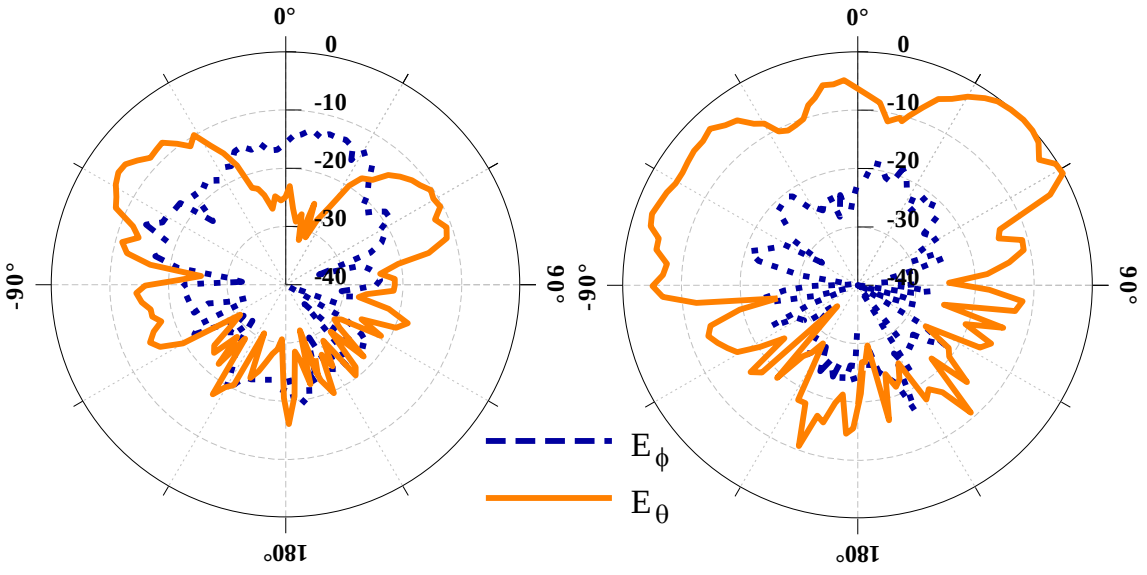

(a) (b)

Figure 35: Simulated radiation patterns for endfire mode for (a) ϕ = 0° and (b) ϕ = 90°.




(a) (b)

Figure 36: Measured radiation patterns for broadside mode for (a) $\phi = 0°$ and (b) $\phi = 90°$.




(a) (b)

Figure 37: Measured radiation patterns for endfire mode for (a) $\phi = 0°$ and (b) $\phi = 90°$.

## 3.3 Summary

In this chapter, the details of monolithically integrated RF MEMS on organic LCP have been discussed. The process has been improved for better reliability. In addition, capacitive RF MEMS switches have been monolithically integrated on multilayer LCP to create a pattern reconfigurable antenna at 30 GHz. The RF MEMS switches have added functionality to the antenna while minimizing negative impact to the antenna pattern.

# CHAPTER 4

# MULTILAYER INTEGRATED PHASED ANTENNA ARRAY

Phased antenna arrays enable beam steering capabilities of directive antenna beams. The directive beam of the antenna array allows longer range and better resolution for applications such as satellite communication, radars, and remote sensing applications. The scanning function of the antenna array, which is enabled by applying a differential phase to the radiating elements, is also essential for these applications. MIMO systems also benefit from phased antenna arrays as a single phased antenna array is used to communicate to multiple targets. Essentially, creating phased antenna arrays reduces the system size, weight, and complexity. Phase shifters are the components that enable variable phase in a phased antenna array. As discussed in Chapter 1, delay line phase shifters offer the most available phase shift as well as the most freedom to create compact devices by meandering the lines. However, the overall size of the delay line phase shifter is still relatively big as the line lengths are dependent on the wavelength. In addition, increasing the number of bits increase the number of lines, which require larger area to incorporate additional lines and bias circuitries. In this chapter, a compact 3D two bit phase shifter is presented that utilizes a SP4T RF MEMS switch. Previous work has shown hybrid integration of RF MEMS switches and LTCC or LCP substrate to create a phase shifter [39], [40]. However, LTCC has limitations in integrating possibilities and the previous work did not put an emphasis on the size of the phase shifter. In this work, the area required for the phase shifter is reduced compared to a single layer layout by taking advantage of the multilayer configuration. RF MEMS switches enable reconfigurable phase states while reducing the required biasing circuitry. In addition, a 2 x 2 phased antenna array is presented that integrates the compact 2-bit phase shifter to show beam steering capabilities.

## 4.1 Multilayer Phase Shifter Design

The side view of the proposed phase shifter is shown in Figure 38. The challenge in designing the phase shifter is to capture the effects of the interconnects and via transitions in the simulation for optimal performance. The input is on the top layer 2 mil above the embedded ground plane. A CPWG to microstrip transition is used for launching the signal from the probes. The ground planes of the CPWG are tied to the embedded ground with 4 mil diameter and 2 mil tall vias. A Radant MEMS SP4T switch is used to vary the phase state. The details of the chip are in [76]. Two SP4T switches are epoxy glued in a 2 mil deep cavity to minimize the height difference between the switch and the substrate for minimal 1 mil gold wirebond length. The lines from the output of the first SP4T switch are routed with $90^{o}$ length difference. Three of the longer states are routed in an embedded layer that is accessed with 8 mil diameter and 4 mil tall vias. The lines are routed underneath the chip cavity and isolated by the ground plane as shown in Figure 39 (b) to maximize compactness. The overall size is 7 mm x 5 mm. In comparison

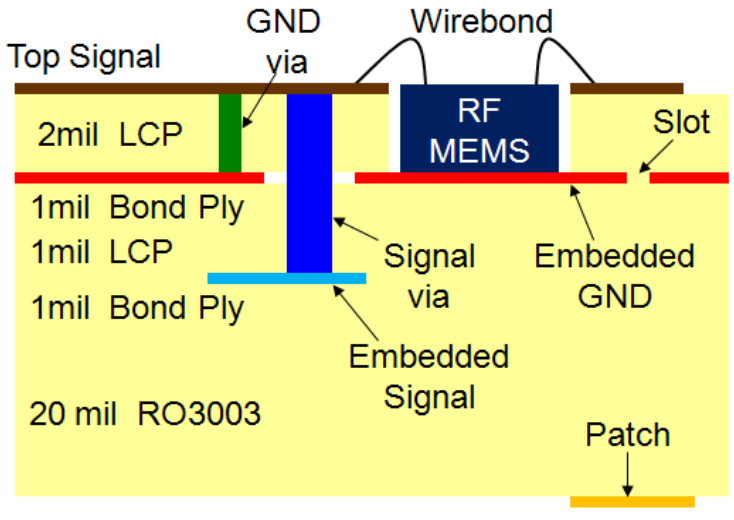
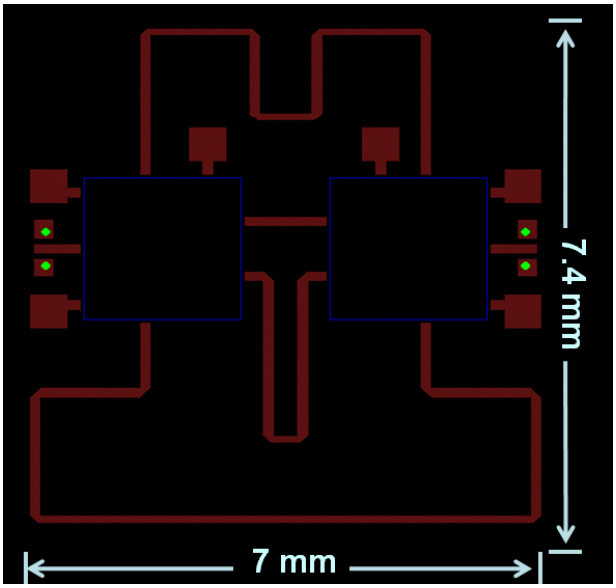
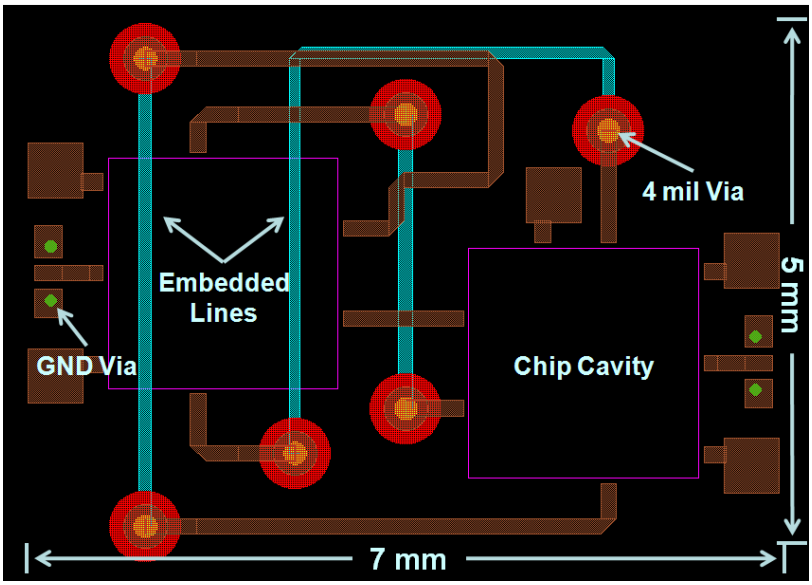



Figure 38: Multilayer stack up of the 3D phase shifter and antenna.




(a)




(b)

Figure 39: Layout view for size comparison of (a) single layer phase shifter and (b) the multilayer phase shifter.

to Figure 39 (a), which shows the layout on a single layer, the multilayer stack up reduces the overall size by 32.4 %. The radiating elements are 23 mil below the ground plane, where a four element antenna array is fed through the slots in the ground plane to create a phased antenna array shown in Chapter 4.2. The signal is coupled from the top layer through the slots to feed the patches.

The delay lines of the phase shifter are given in $90^o$ phase increments where each line length is estimated by (14).

$$l_n = l_o + n \cdot \frac{\lambda}{4} \tag{14}$$

where $l_n$ is the length of the nth line in reference to $l_o$ (the $0^o$ line) and n refers to the 90•no line. λ is the wavelength on LCP, which is approximately 17.3 mm at 10 GHz. The $90^o$ phase difference among elements gives the maximum beam steer for antenna arrays with λ/2 spacing, which is most common. Once the estimated line length is calculated, ADS Momentum is used to further optimize the design to include the effects of bends, wirebonds, and via transitions.

Figure 40 shows the simulated 3D phase shifter S-parameter response without the SP4T switch and wirebonds. The average line loss is 0.18 dB at 10 GHz with a return loss better than -25 dB return loss. The data sheet [76] shows that the SP4T switch adds an average of 0.35 dB while the phase of each state is assumed to be equal. Assuming 0.3 dB of loss from the wirebonds, the total expected average loss is 1.2 dB. Figure 41 shows the simulated phase where each state has approximately $90^o$ phase difference.

The assembled 3D phase shifter is shown in Figure 42. The measured S-parameter response is shown in Figure 43. The average insertion loss is 1.44 dB that translates to 0.72 dB per bit at 10 GHz with better than -12 dB of return loss. The amount of loss from

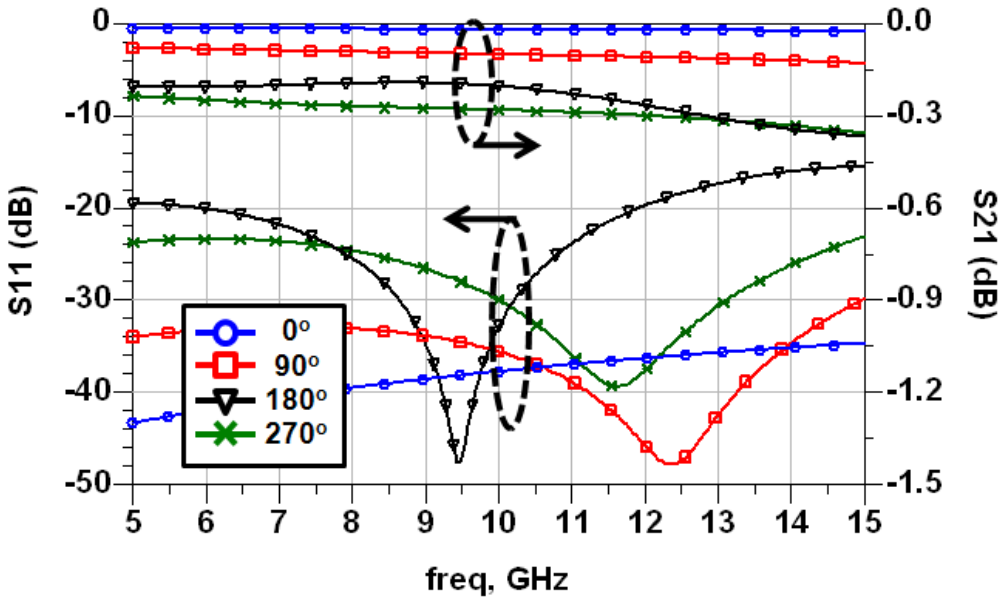



Figure 40: Simulated reflection and insertion loss of the 3D phase shifter.

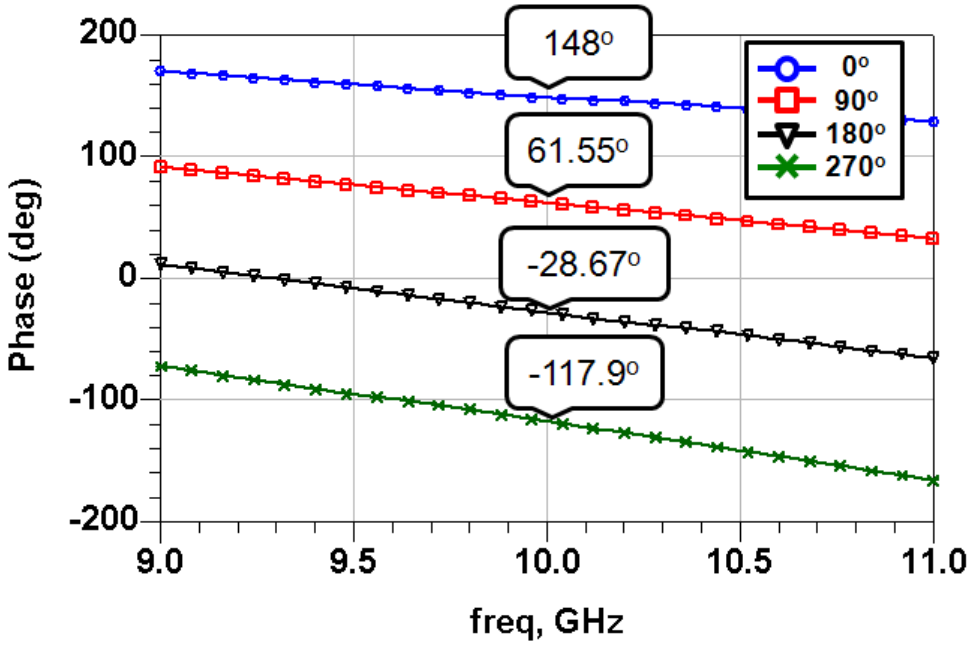



Figure 41: Simulated phase response of the 3D phase shifter.

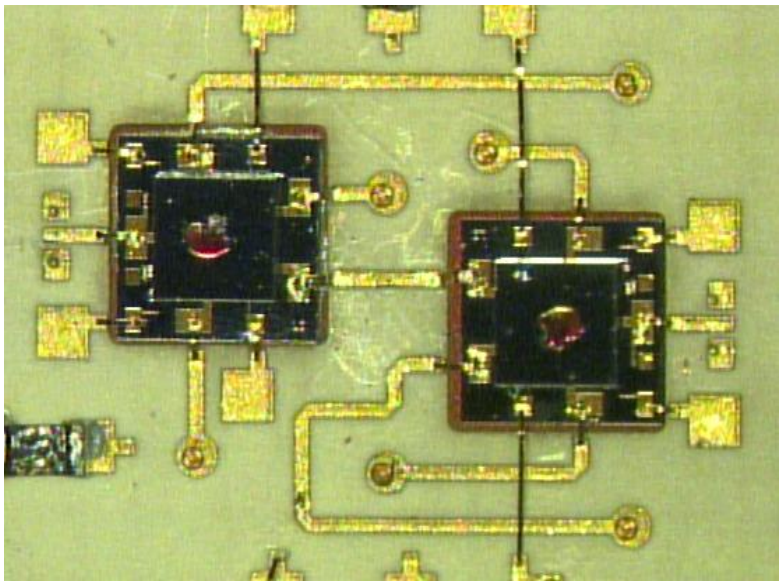


Figure 42: Assembled 3D phase shifter.

each phase state increase according to the line length as expected. The actuation voltage is 70 V but 85 V is applied to increase the contact force for a good response. The additional loss in comparison to the simulated values is attributed to the fabrication tolerances and the loss assumptions made in the simulations as well as for the wire bonds. The measured phase response is shown in Figure 44. The average phase error is 1.13$^{o}$, which is very small for a delay line phase shifter.

A compact multilayer phase shifter has been designed, fabricated, and measured. The overall reduction in foot print compared to a single layer layout is 32.4% while maintaining a low loss performance with minimal phase error. In the next chapter, these phase shifters are used to control a 2 x 2 phased antenna array for beam steering applications.

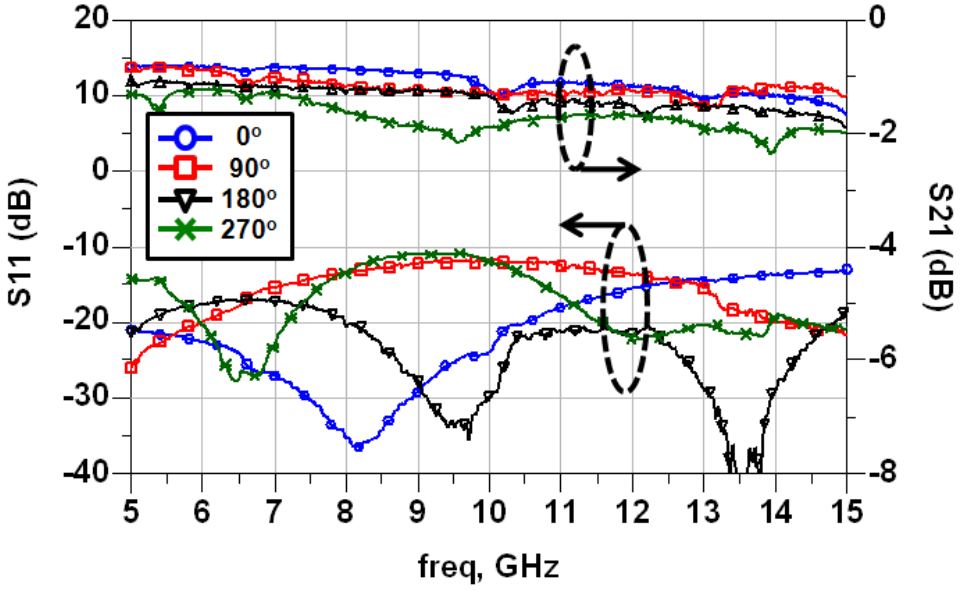



Figure 43: Measured reflection and insertion loss of the 3D phase shifter.

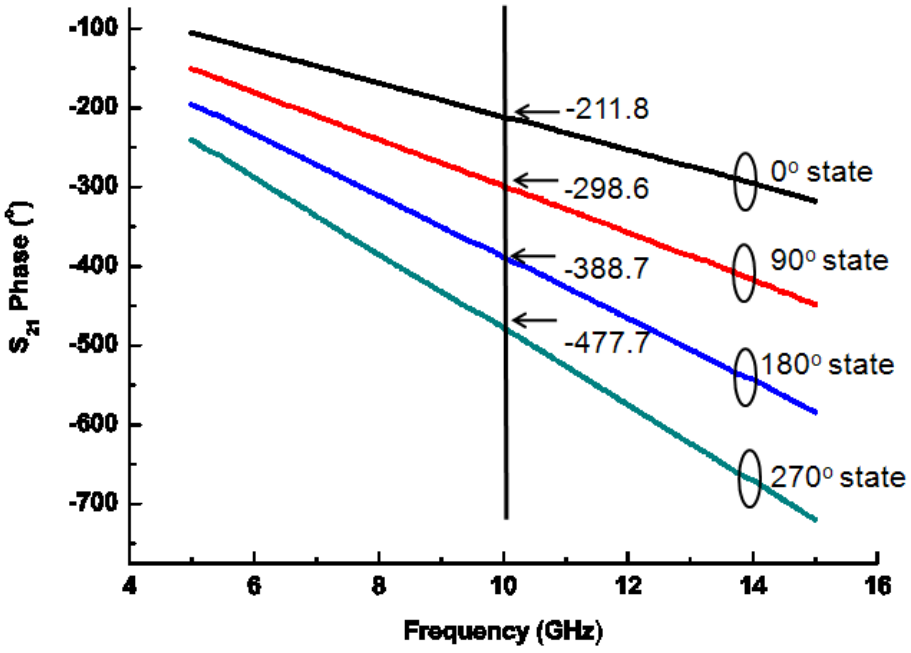
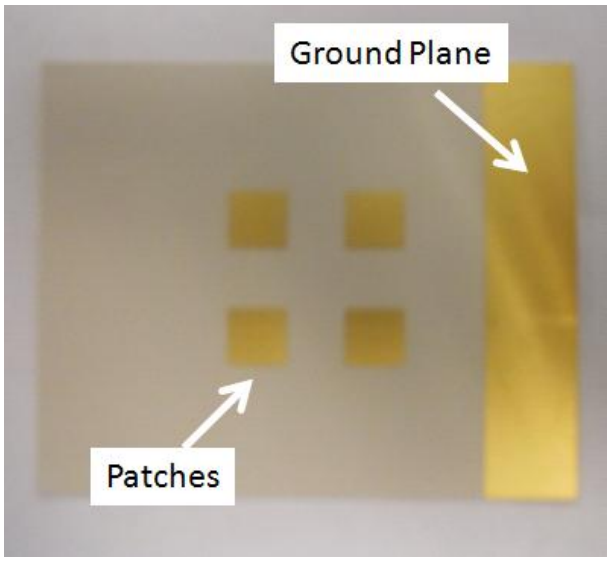



Figure 44: Measured phase response of the 3D phase shifter.

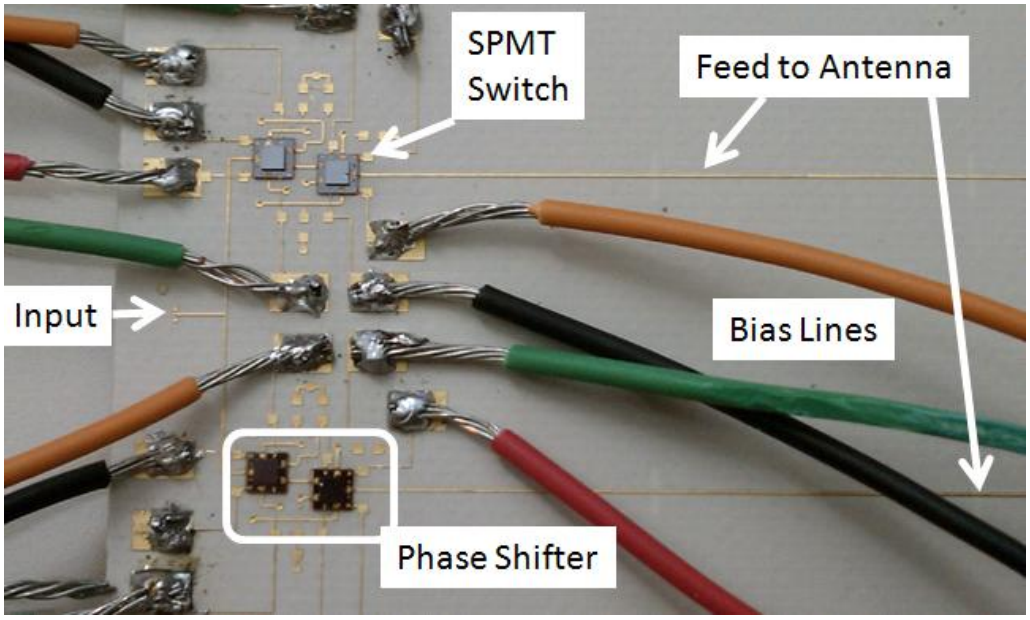
## 4.2 2 x 2 Multilayer Phased Antenna Array

Using the compact 3D phase shifters shown in the Chapter 4.1, a 2 x 2 phased antenna array is assembled as shown in Figure 45. The multilayer stack up is the same as the previous chapter shown in Figure 38. Figure 45 (a) shows the patch layer that has a floating ground plane for measurement purposes and four patches with a size of 7.9 mm by 8.1mm. The vertical edges are shorter because of the fringing field effects of the electric field. Figure 45 (b) shows the feed line layer including the top of the 3D phase shifter. The input is a CPWG for probe feed and transitions into microstrip mode. The signal is then split into two and quarter wavelength transformers are used to maintain 50 ohm lines. The signal then goes through the phase shifter that routes the signal through the corresponding delay line for desired phase state. The DC bias lines are soldered on to metal pads that connect to the SP4T chips with wirebonds. The output of the phase shifter is a long microstrip line that feeds two patches in series. Thus, the beam steering is enabled in the H-plane while the *E*-plane remains constant.

The measured $S_{11}$ response of the $0^o - 0^o$ state is shown in Figure 46 compared to the simulated $S_{11}$ response. A small shift of the resonance frequency is observed that is attributed to fabrication tolerances. Figure 47 shows the measured $S_{11}$ of a $90^o - 0^o$ state along with the measured $S_{11}$ when a metal plate is placed in the vicinity of the patches. This is done to ensure that the patches are radiating by observing the resonance disappear as in Figure 47. The resonance disappears because the radiated signal sees a metal plane and it is reflected back to the source. The additional resonances other than the radiating resonance are internal resonances that do not affect the radiation.


Ground Plane
Patches

(a)


SPMT
Switch
Feed to Antenna
Input
Bias Lines
Phase Shifter

(b)

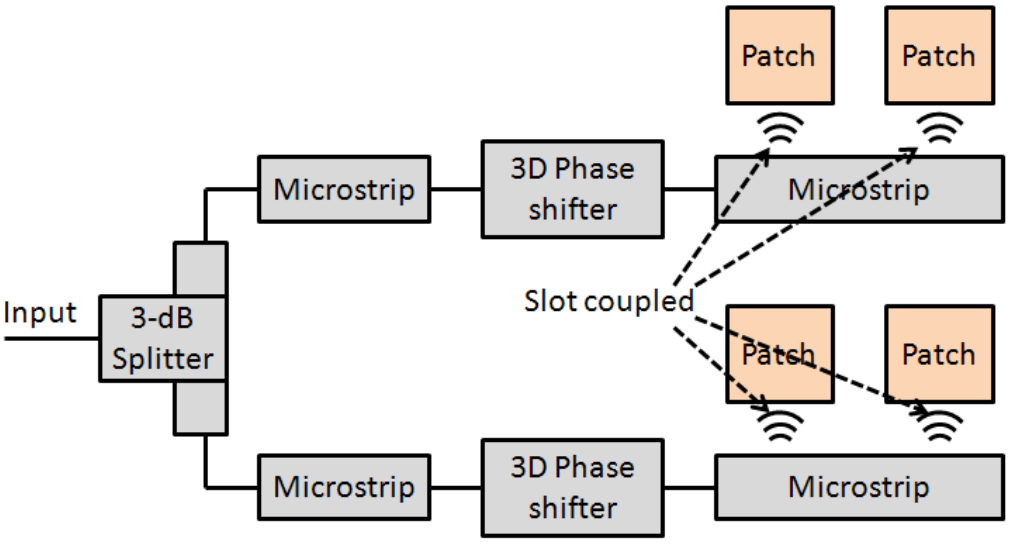



Figure 45: Assembled 2 x 2 phased antenna array (a) patch layer with 7.9 mm x 8.1 mm patches (b) feed line layer with two phase shifters that control two radiating elements (c) block diagram.

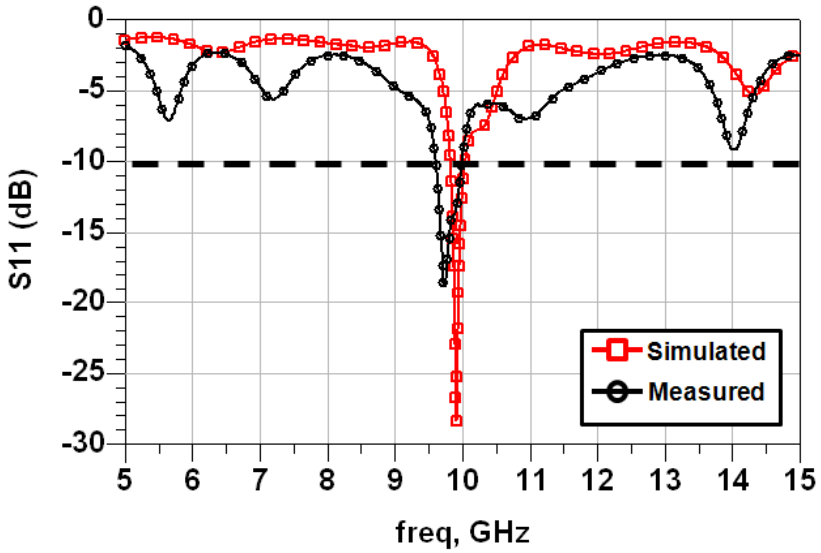



Figure 46: Measured and simulated return loss of the 2x2 antenna array with no phase difference applied.

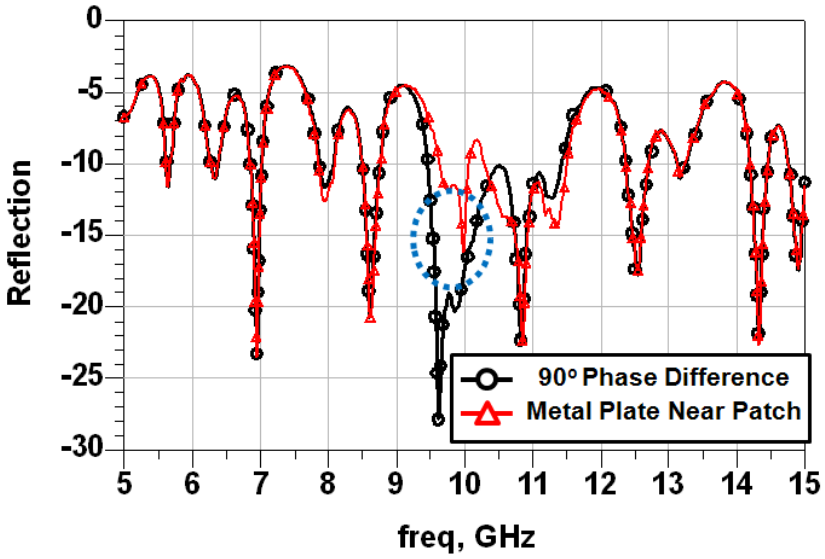



Figure 47: Measured return loss of the 2x2 antenna array with $90^{o}$ phase difference on the two phase shifters. A metal plate is placed near the patches to confirm the radiation.

The simulated radiation response is shown in Figure 48. The $0^{o} - 0^{o}$ state shows a broadside mode radiation with a maximum gain of 9.4 dBi and a 3 dB beam width of $24^{o}$. By applying a phase difference in the phase shifters, the main beam is steered $8^{o}$ in either direction with a 0.8 dB drop in gain. The measured radiation pattern are normalized and shown in Figure 49 with varying phase states of the two phase shifters. The maximum of the $0^{o} - 90^{o}$ and $90^{o} - 0^{o}$ states are $11^{o}$ away from the azimuth. However, the $0^{o} - 0^{o}$ state itself shows a tilted beam that does not point towards the azimuth. This may be due to the bias lines adding interference as well as other simulation assumptions such as a perfect line in place of the wire bonded phase shifters. Another major factor is from the imperfect performance from the integrated Radant RF MEMS switches. The switches did not yield reliable results as the switches shorted many times during the integration and measurements. However, the concept of the beam steering is seen in comparison to the

$0^{o}$– $0^{o}$ state. The recommended cold switching (RF power off when actuating) of the RF MEMS switches limits the possible applications that would benefit from these switches.

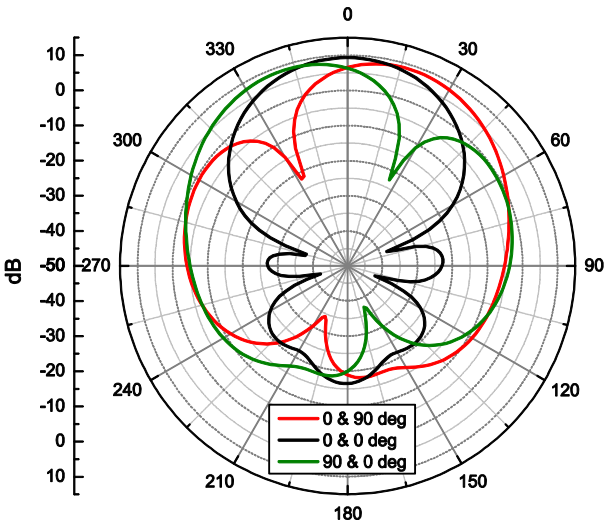



Figure 48: Simulated antenna radiation pattern with varying phase states.

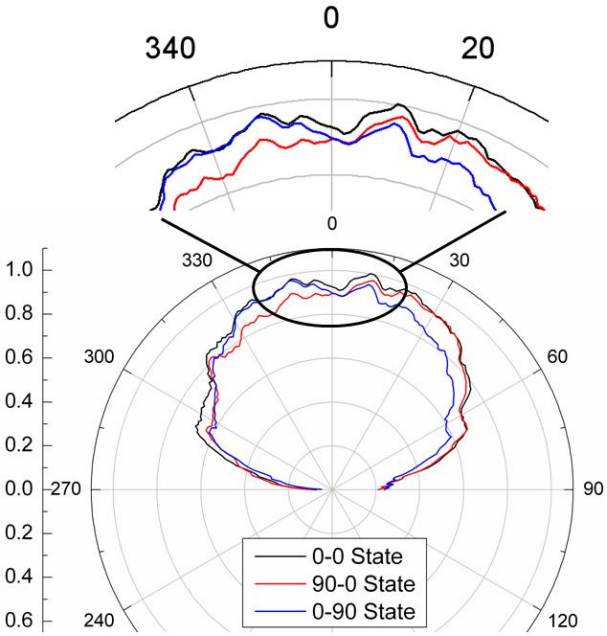


Figure 49. Normalized measured radiation pattern of the 2 x 2 antenna array with varying state.

## 4.3 Summary

In this chapter, a compact 3D phase shifter and a 2 x 2 phased antenna array are designed, fabricated, and measured. A 32.4 % overall size reduction is achieved by routing the lines on multiple layers. The compact phase shifter exhibits 0.72 dB of loss per bit and $1.13^{o}$ of average phase error. The beam steering concept has been demonstrated and more reliable RF MEMS switches for integration are presented in the next chapter.

# CHAPTER 5

# LOW VOLTAGE PZT RF MEMS

Electrostatic RF MEMS switches are attractive because they are easy to integrate, have a simple design, and have a relatively small size. However, the biggest problem for integration is the high actuation voltage. This chapter discusses a solution to this problem. In contrast to the Chapter 4, low voltage PZT MEMS switches are used to design a more compatible phase shifter for integration with various IC components. A compact 3D phase shifter is designed, fabricated, and measured. The phase shifter is configured in a multilayer stack up to reduce the footprint of the device.

## 5.1 PZT Switches

Typical active devices in a communication module operate in the order of 3 – 5.5 V. Most electrostatic RF MEMS switches require a voltage above 30 V. This is a problem for achieving compact integration for several reasons. First, a high voltage component needs multiple stages of components to increase the voltage to reach the high voltage, which in turn consumes more power and requires additional biasing circuitry offsetting the benefits of a near-zero power MEMS switch. Secondly, additional isolation is needed to protect other components from the high DC voltage as the DC voltage can couple over to other lines and cause system failure. Finally, the additional components and space required rapidly increases the overall size of the system. To integrate lower actuation voltage RF MEMS switches, ohmic PZT switches are investigated. PZT MEMS switches actuate well below 20 V and the lowest voltage reported is 2 V. Individual PZT switches, shown in Figure 50 have been designed at the US Army Research Laboratory (ARL) with an actuation voltage of 7 V and a dimension of 230 µm x 200 µm. The switches show great RF characteristics, greater than 20 dB isolation and less than 0.5 dB

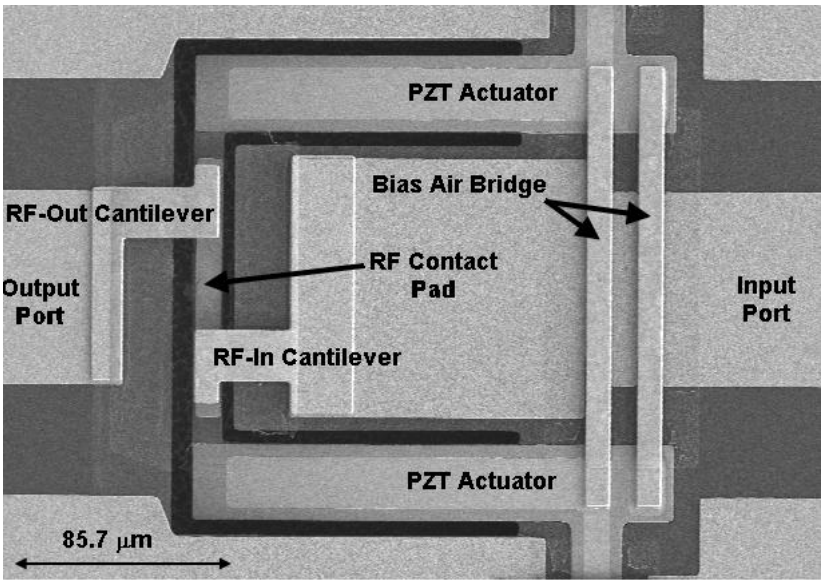
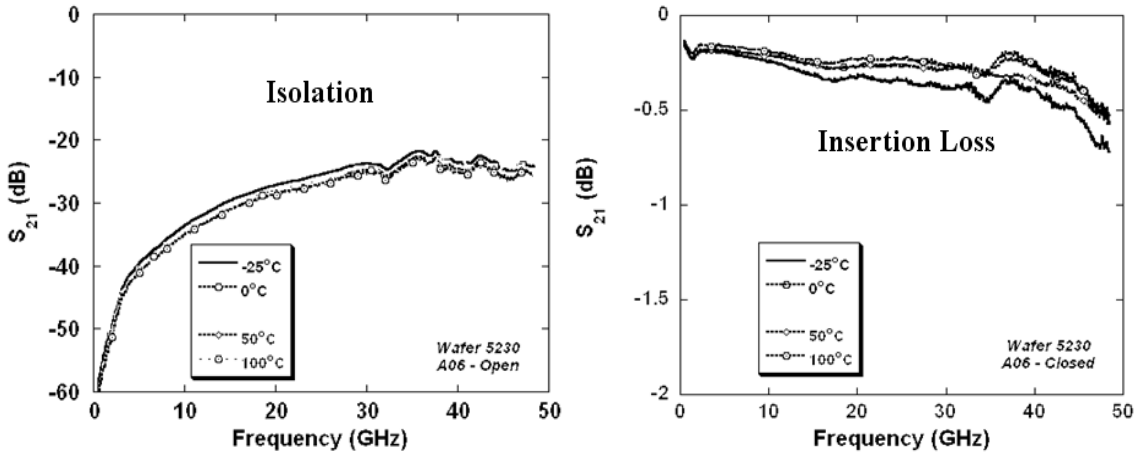



Figure 50: Fabricated single PZT MEMS switch.




(a) (b)

Figure 51: Measured response of PZT MEMS switch (a) $S_{11}$ (b) $S_{21}$.

of loss up to 50 GHz as shown in Figure 51. The fabrication is carried out at the US ARL cleanroom facility. Starting with the seed layer of patterned Pt and PZT, the structural layer is patterned. Next, ion etching is used to expose the silicon for the eventual release etch. The CPW lines are patterned and the contact dimple is made for minimal contact

area. Then, the sacrificial layer is patterned followed by the bridge layer. $O_2$ plasma is used to remove the sacrificial layer and $XeF_2$ is used to remove the silicon underneath the actuators. The bulk of the fabrication procedure is explained in detail in an earlier publication [43]. The only significant change in the fabrication process involves altering the sacrificial photoresist layer to enable a liftoff procedure to pattern the gold used for the air bridges and cantilevers. It should be noted that the open cavities near the switch junctions are created with the same $XeF_2$ etch step that releases the PZT actuators. The measured response of the PZT MEMS switch is shown in Figure 51. The actuation voltage is 7 V with an insertion loss lower than 0.5 dB and return loss better than -20 dB up to 40 GHz. These individual switches are used in the design of a SP2T and a SP4T shown in Figure 52. The overall size of the final Single Pole Multi Throw (SPMT) design is 1.6 mm x 2.2 mm. The signal line width is 75 μm and the optimal simulated performance came with a spoke width (the line width in the spoke region) of 27 μm. All bends in the circuit have been optimized for the best impedance match ranging from 20 to 25 μm. In addition, there are 15 μm air bridges across all of the bends and discontinuities in the CPW line, and also along the 5 μm actuator bias lines. The air bridges are for suppressing extra modes that can rise from the discontinuities by connecting the ground planes.

The measurement of the S-parameters is carried out using an Agilent E8361A vector network analyzer from DC to 50 GHz. The SP2T in Figure 52 (a) has one input and two PZT MEMS switches leading to the outputs. The SP4T has one input and four PZT MEMS switches leading to outputs. In both cases, any given path will require one PZT MEMS switch to operate. The difference between Figure 52 (b) and Figure 52 (c) is that (b) does not have an undercut in the spoke region and has a spoke width of 27 μm. The spoke region in (c), marked with a circle and arrow, has the silicon removed beneath it and the spoke width is widened to 35 μm. The undercut decreases the effective capacitance as the silicon is removed and replaced with air, thereby, allowing wider

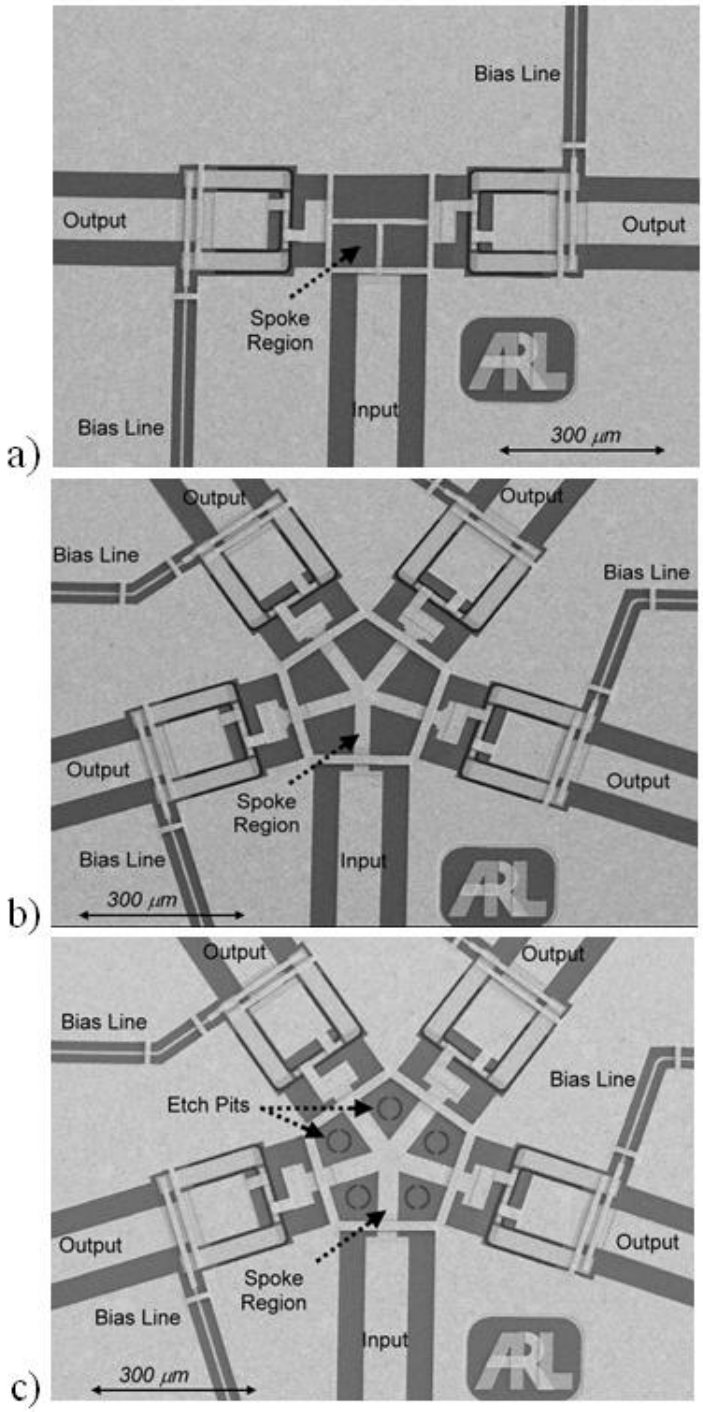



Figure 52: Fabricated SPMT switches (a) SP2T, (b) SP4T, and (c) SP4T with etch pitches.

transmission lines in this region for greater power handling capabilities.

Figure 53 shows the measured response of the SP2T switches. The isolation is greater than 20 dB from DC to 50 GHz for both the $S_{21}$ and $S_{31}$ responses. There is less than 2 dB of loss up to 40 GHz with an actuation voltage of 7 V. A DC current of 100 mA is sent through the circuit to break through any residue that may be left on the contact point. The PZT switches have introduced parasitic capacitance and inductance as well as contact resistance that have not been accurately modeled in the initial simulations. Including accurate models of MEMS switches lead to memory problems and time consuming simulations that have been replaced with ideal modeling of the MEMS switches.

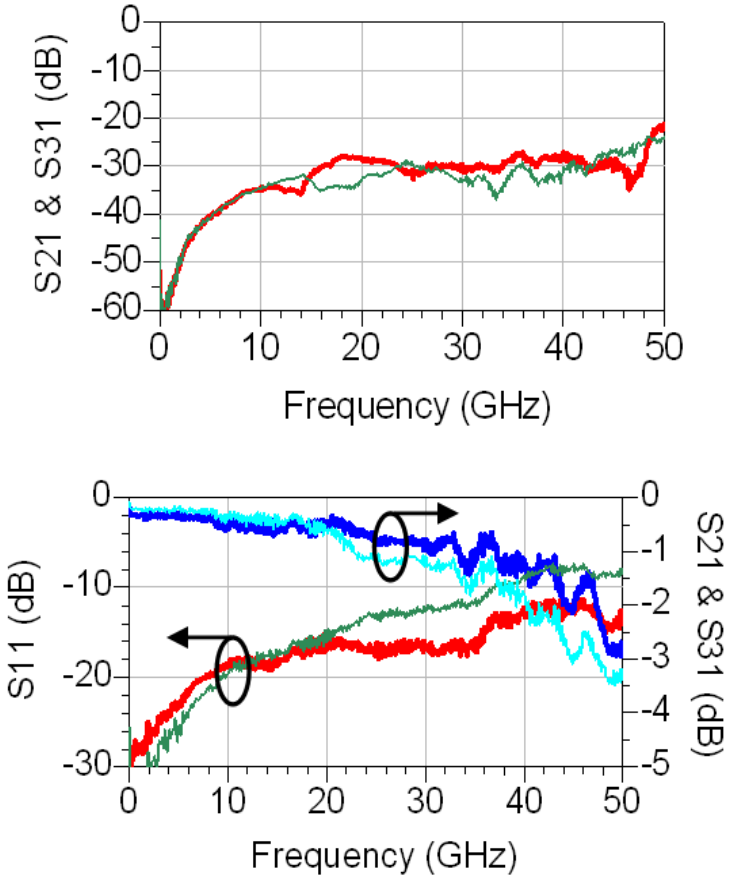



Figure 53: Measured isolation (top), insertion loss, and return loss (bottom) of SP2T.

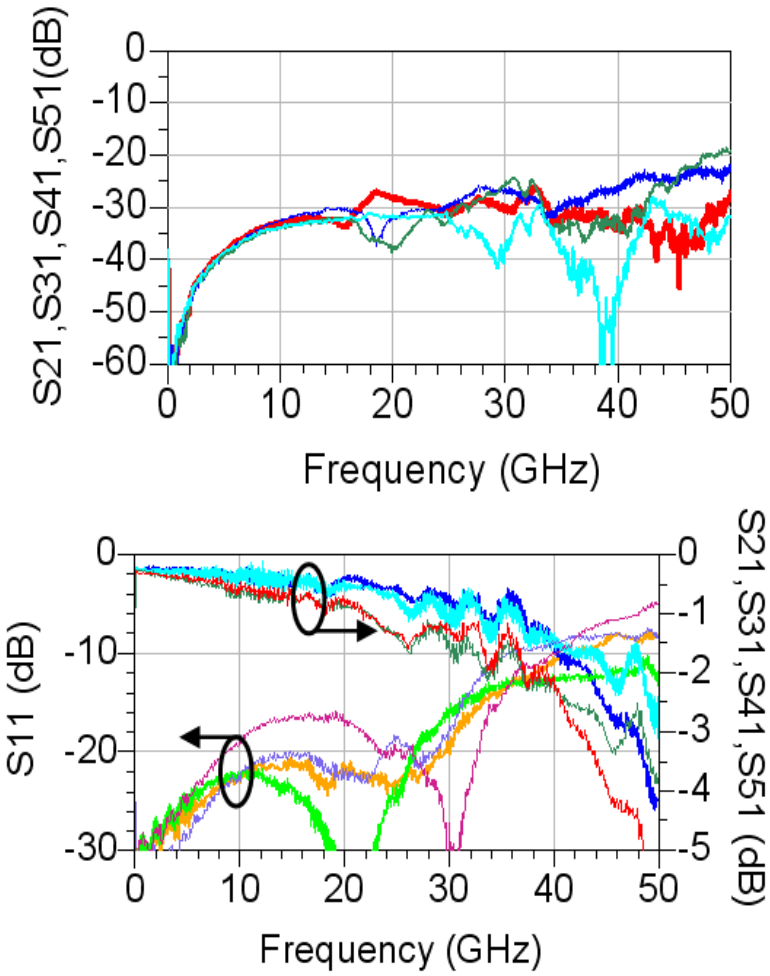



Figure 54: Measured isolation (top), insertion loss, and return loss (bottom) of SP4T.

The measured response of the SP4T design is shown in Figure 54. The isolation is greater than 20 dB up to 50 GHz similar to that of the single switch. On average, the insertion loss is less than 1 dB at 20 GHz and about 2 dB at 40 GHz. The return loss is greater than 15 dB up to about 30 GHz. Similar to the SP2T switch, the SP4T does not exhibit a great match at higher frequencies in contrast to the modeling predictions. Comparing to the simulated and estimate results, we have an additional 0.5 dB of loss to account for. Possible reasons include contact contamination from the fabrication process and discrepancies between the simplified simulation and the actual switch response. The additional loss is not a big deviation from the measured results and the overall response is

well estimated with the simulations. Figure 55 shows the measured response with and without the undercut that is shown in Figure 52(c). The darker colors represent the original measurement and the lighter colors show the response after the undercut. There is only a slight drop in the overall performance while being able to widen the spoke region to provide better RF power handling.

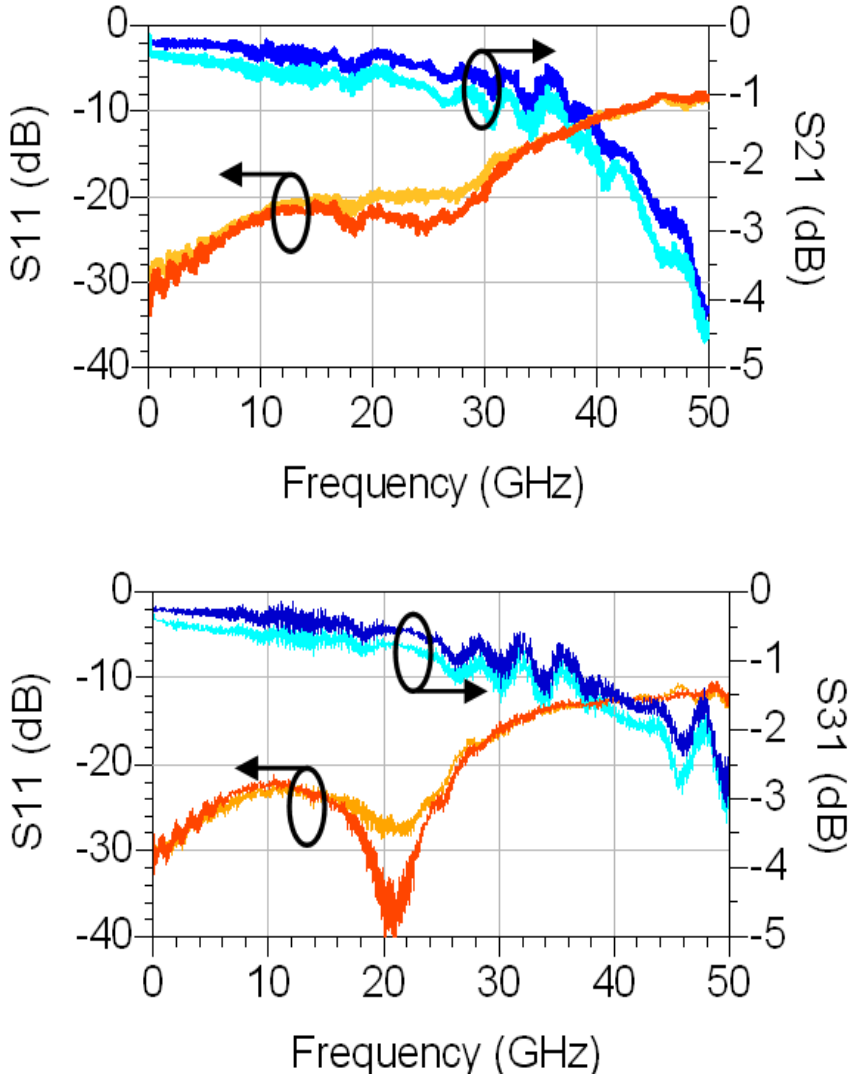



Figure 55: Measured SP4T response with (light) and without (dark) under cut. (top) port 2 actuated (bottom) port 3 actuated.

Low voltage PZT RF MEMS switches have been successfully implemented to create SP2T and SP4T switches. With an actuation voltage of 7 V, the SPMT junctions show less than 2 dB of loss up to 40 GHz. In addition, a variation of the SP4T junction that allows more power handling capability has been shown. This is the first time to show SPMT switches using PZT MEMS switches that requires less than a 10 V actuation voltage.

## 5.2 Compact Multilayer Phase Shifter

The SP4T junction with the PZT switches from Chapter 5.1 is used to create a compact low voltage phase shifter. The phase shifter from Chapter 4 actuates at 85 V, which can cause failure in a system if coupled over to an IC chip. Proper isolation and protection from this high voltage requires additional components and may complicate the routing of the DC bias lines. Thus, a low voltage phase shifter that actuates under 10 V is advantageous for integration purposes. In addition, by routing the lines on different layers as the previous chapter, the size is minimized. Figure 56 shows the top view of the proposed multilayer phase shifter with integrated PZT SP4T switches and the layout of a single layer phase shifter. In comparison to a single layer layout, the multilayer design shows a 22.5 % reduction in foot print. The size of the multilayer design is 9.5 mm x 4.8 mm, which includes two 1.6 mm by 2.2 mm SP4T junctions. The cavities are oversized to account for chip size and cavity size variations. The delay lines of the phase shifter are given in $90^{o}$ phase increments for maximum beam steer for the most common $\lambda/2$ spacing antenna arrays. ADS and HFSS are used to optimize the design to include the effects of bends, 1 mil wirebonds, and via transitions.

The lines on LCP are Grounded Co-Planar Waveguide (CPWG) lines to match the CPW lines on the SP4T chip. The embedded lines however, are microstrip lines, requiring simple CPWG to microstrip transitions. The embedded microstrip lines are mitered at the bends and the width needs to be optimized to compensate for the additional

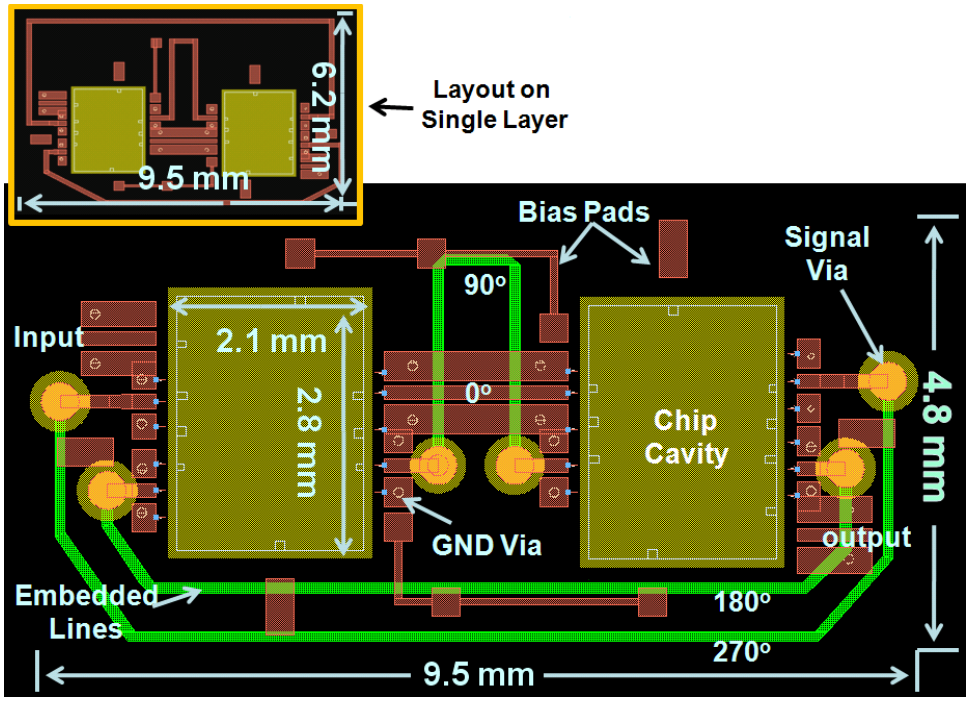



Figure 56: Layout of 3D phase shifter with size comparison to a single layer phase shifter.

parasitic capacitance and inductance from the via transitions. Figure 57 (a) shows the stack up and Figure 57 (b) shows the equivalent block diagram of the multilayer design. The bond ply material has the same electric properties but a lower melting temperature (285 $^{o}$C) compared to the core LCP (315 $^{o}$C), which allows the bonding of multilayer stack up. The 20 mil RO3003 is an organic material with similar electrical properties that is chosen for the purpose of creating a cavity and embedded layers. The ground vias are 4mil diameter and the signal vias are 8 mil diameter with a diameter to height ratio of 2:1. The landing pad for the signal via is 16 mil diameter and the anti-pad in the embedded ground is 24 mil diameter to give 4 mil around each circle for fabrication tolerances. The silicon PZT SP4T chips are 21 mil thick and they are mounted in a cavity with silver epoxy and wirebonded out to the top signal lines. In addition, the chips are placed on a small piece of 4 mil LCP to level the SP4T chip surface to the top signal layer on LCP for minimal wirebond length.

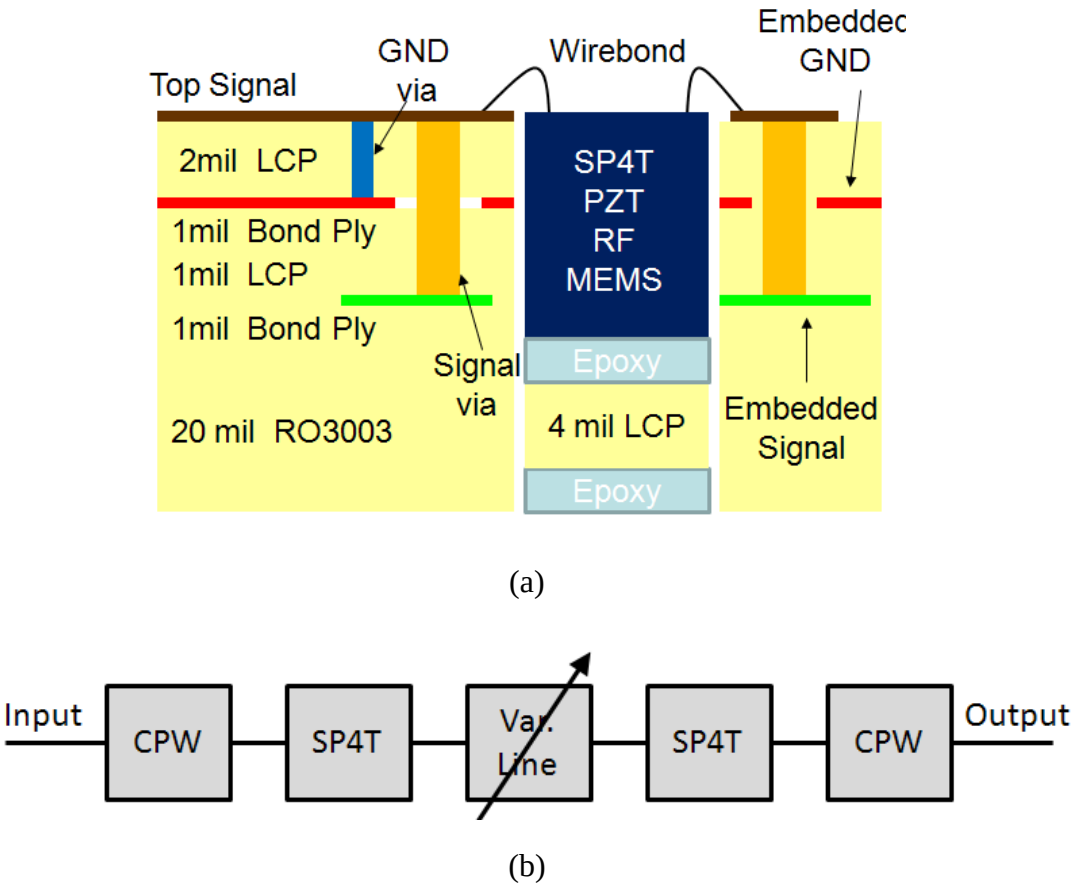



Figure 57: The 3D phase shifter design (a) stack up and (b) block diagram representation.

Figure 58 shows the simulated response of the phase shifter assuming 500 µm wirebonds and the measured SP4T chips. The return loss is greater than 13 dB and the average insertion loss is 1.3 dB. Figure 59 shows the simulated effect of the wirebond length with the overall phase shifter response degrading with increasing wirebond length especially above 11 GHz.

The LCP multilayer design is processed on a 12 inch by 18 inch panel with 75 µm minimum features. The fabricated and assembled 3D phase shifter is shown in Figure 60. One mil wirebonds are used to connect the SP4T chip to the lines on LCP. Though the PZT MEMS actuate at 7 V, a 10 V bias is used for actuation to achieve a higher contact force, which improves the insertion loss. Higher contact force results in a lower contact resistance for the ohmic contacts.

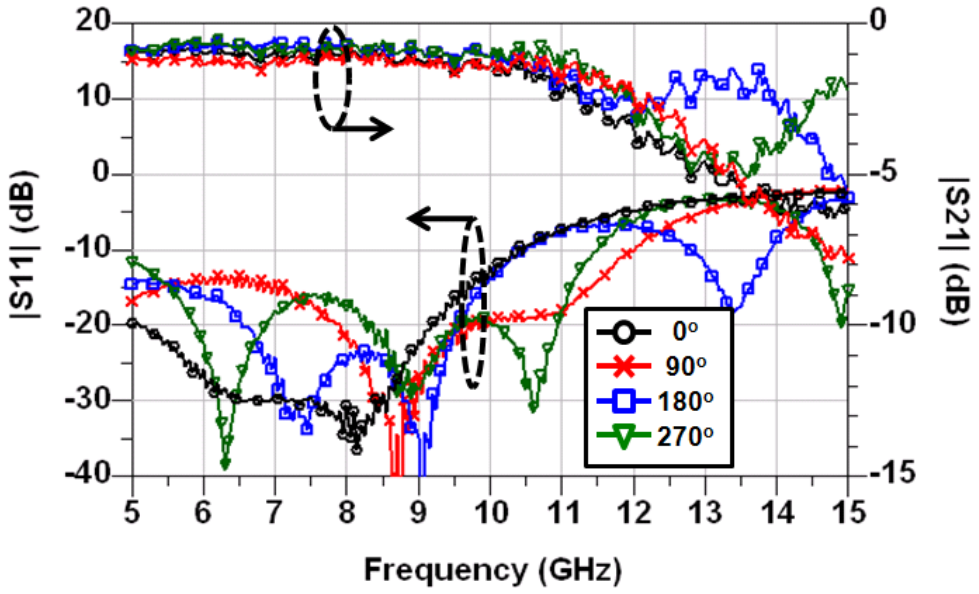



Figure 58: Simulated phase shifter response with measured SP4T switches.

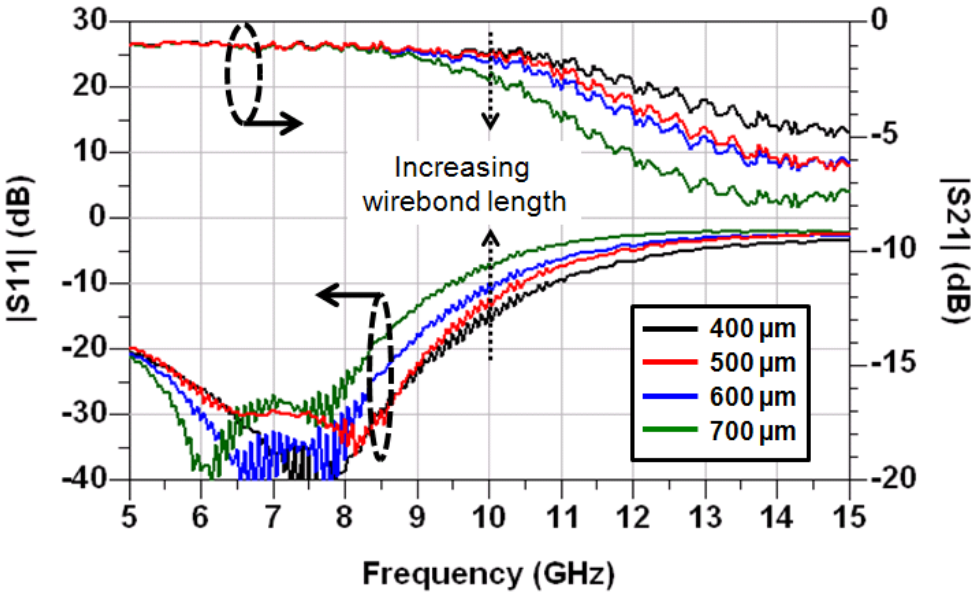



Figure 59: Simulated $0^{o}$ state with increasing wirebond lengths.

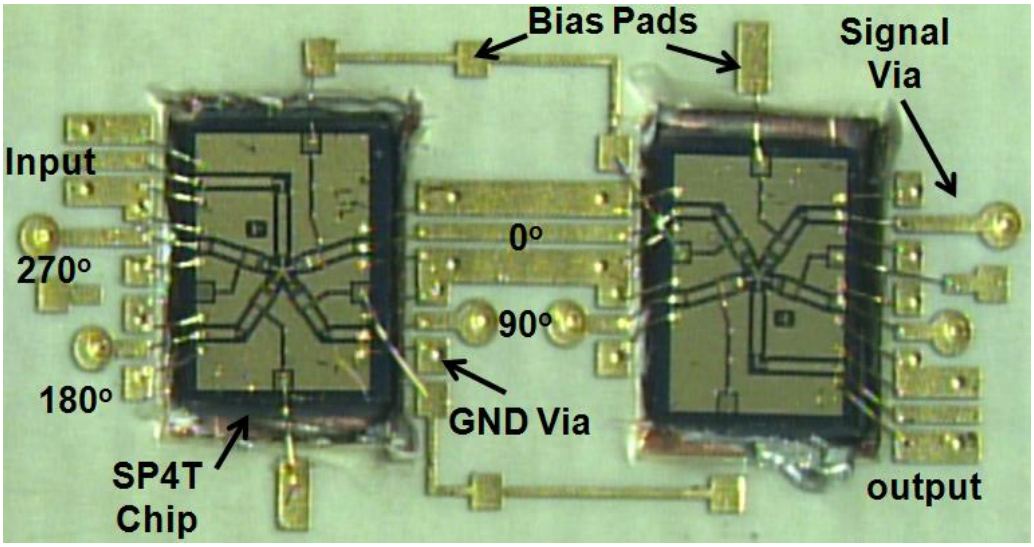



Figure 60: Fabricated and assembled device.

Figure 61 shows the measured return loss and insertion loss of the 3D phase shifter. At 10 GHz, the worst case is the longest phase line with 1.66 dB of loss and the best case is the shortest phase line with 1.17 dB of loss. On average, the line loss is 1.5 dB, which amounts to 0.75 dB/bit. The return loss shows that the device is well matched at 10 GHz with better than -18.3 dB. The performance of the phase shifter above 11 GHz declines though the SP4T switch and via transitions have wide band performance beyond 20 GHz. It is suspected that the degradation results from several wirebonds measuring in excess of 600 µm. As the frequency increases, the effective parasitic resistance and inductance of the thin wirebonds increase as well, resulting in higher loss and worse matching. Reducing the length or using thicker wirebonds, preferably ribbon bonds can help improve the performance at higher frequencies. The measured phase response for each $90^{o}$ incremental state is shown in Figure 62. The average phase error for each state in reference to the $0^{o}$ state is $2.25^{o}$. The $90^{o}$ state shows unexpected resonances above 11 GHz which may be the result of poor contact resistance in one state of the PZT switch. The performance of the phase shifter is summarized in Table 5.

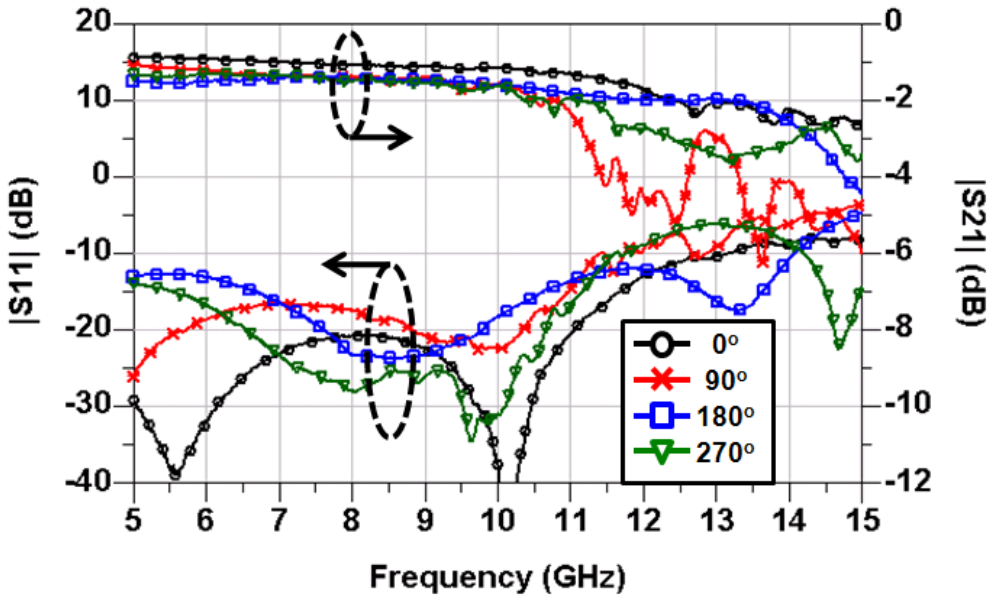



Figure 61: Measured S-parameters of the 3D phase shifter.

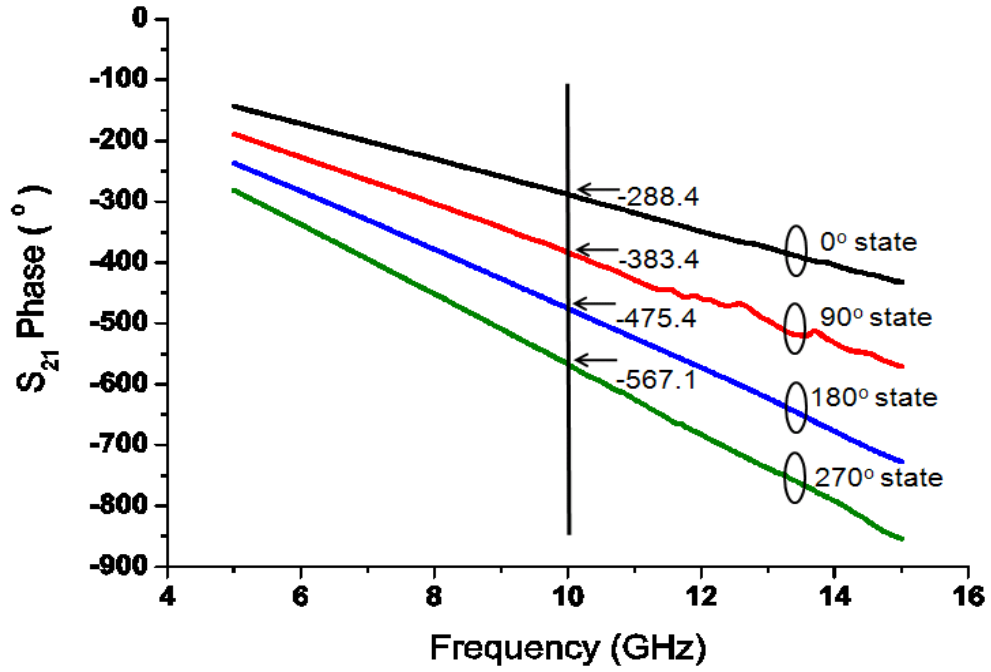



Figure 62: Measured phase response.

The loss and size can be further improved by reducing the overcompensated size of the cavity, which leads to shorter wirebonds with less parasitic effects. In addition, if the SP4T switches are made application specific, the size of the MEMS chip can be reduced in half so that the cavity size is further reduce and the line loss on chip decreases. The result of these corrections leads to at least another 15% additional reduction in size and more than 0.3 dB improvement in insertion loss.

TABLE 5
SUMMARY OF PHASE SHIFTER PERFORMANCE AT 10 GHZ

| | Worst Case | Average | Best Case |
|---|---|---|---|
| Simulated S21 (dB) | -1.39 | -1.22 | -1.04 |
| Simulated S11 (dB) | -18.95 | -21.86 | -23.6 |
| Measured S21 (dB) | -1.66 | -1.5 | -1.17 |
| Measured S11 (dB) | -18.3 | -20.4 | -31 |
| Phase Error ($^{o}$) | 4.85 | 2.25 | 1.69 |

## 5.3 Summary

In this chapter, low voltage PZT RF MEMS switches have been used to first design SP2T and SP4T junctions, in which the SP4T junctions are used to design a compact multilayer phase shifter. This is the first work to design low voltage SPMT junctions with PZT RF MEMS switches as well as the first attempt to integrate PZT MEMS switches with organic LCP to create a 3D phase shifter. The phase shifter operates with 10 V, which is comparably better than electrostatic actuated RF MEMS switches for integration with IC components. In addition, a 22.5 % reduction in the overall size is achieved compared to a single layer layout.

# CHAPTER 6

# PHASED ANTENNA ARRAYS ON MULTILAYER LCP

Multilayer integration becomes necessary as increasing functions and higher transmitting power are required for emerging communication applications. In general, more components are needed in the advancing communication systems with less real estate available. In a simple 2D configuration of the system, the active components, feeding network, and other passive components easily crowd the layout to interfere with the radiating elements that degrades the overall performance. Multilayer integration, or 3D integration, offers the advantages of isolating the components in the system to reduce the mutual coupling and decrease unnecessary radiations while reducing the overall size. Despite these advantages, the overall size and weight, the loss on the lines, and fabrication difficulties remain as a major challenge for large antenna arrays. Designing microstrip antenna arrays on lightweight, low loss, multilayer LCP offers a solution to these challenges. Microstrip antennas are less efficient compared to aperture antennas or other high gain antennas, but they are significantly lighter, smaller, and simpler [77], [78]. In addition, microstrip antennas are easier for integration purposes on multilayer stack ups. In this chapter, microstrip patches are designed for phased antenna arrays with up to 256 elements that are built on multilayer LCP for satellite applications. Overcoming the fabrication capabilities and simulating the effects of the large scale integration are the key challenges in this chapter.

## 6.1 Background of Phased Antenna Array

Antenna arrays are used for long distance or high power communications where a high gain/directivity is desired. The directivity is estimated with the 3-dB beam widths by the following equation (15),

$$D_o \approx \frac{22.181}{\Theta_{1r}^2 + \Theta_{2r}^2} \ , \tag{15}$$

where $D_o$ is the maximum directivity and $\Theta_{1r}$ and $\Theta_{2r}$ are the 3-dB beamwidths in radians of the E- and H-planes [35]. A higher directivity is achieved with a narrower beam. The ideal gain of an antenna array is estimated from the following equation,

$$G = \varepsilon_{ap} \frac{4\pi}{\lambda^2} A_p = \varepsilon_{ap} \frac{4\pi}{\lambda^2} L_x L_y = \varepsilon_{ap} \frac{4\pi}{\lambda^2} \left(\sqrt{N}d\right)\left(\sqrt{N}d\right) = \varepsilon_{ap} \frac{4\pi}{\lambda^2} Nd^2 \ , \tag{16}$$

where $\varepsilon_{ap}$ is the efficiency, $A_p$ is the area of the aperture, N is the number of elements, and d is the antenna element spacing [79]. The gain is increased by increasing the number of elements or increasing the element spacing. However, increasing the spacing is not the ideal way to go about improving the gain as the array size increases and secondary lobes occur in the pattern. The gain increases proportionally to the number of elements, in which by doubling the number of elements, a 3-dB increase in gain is expected.

For an N element, uniform, equally spaced linear array the normalized array factor is given by [79]

$$f(\Psi) = \frac{\sin(N\Psi/2)}{N\sin(\Psi/2)}, \tag{17}$$

where

$$\Psi = \alpha + \beta d\cos\theta \, . \tag{18}$$

$\alpha$ is the phase difference given to each array element, $\beta$ is $2\pi/\lambda$, d is the spacing between the array elements, and $\theta$ is the angle of the main beam from the azimuth. A maximum occurs when $\psi = 0$ resulting in

$$\alpha = -\beta d\cos\theta \, . \tag{19}$$

Thus, by applying an inter-element phase $\alpha$, the main beam is steered by an angle $\theta$ for scanning. In the case of planar arrays, the phase $\alpha$ two components $\alpha_x$ and $\alpha_y$ that allows a beam steer in both the x-direction and the y-direction. In this chapter, N x M element, uniform, $\lambda/2$ spaced planar arrays are presented.

## 6.2 4 x 8 Antenna Array

Using via technology and bonding of LCP layers, a 3D 4 x 8 patch antenna array is designed with an operating frequency of 14 GHz for satellite observation of precipitation. By using multilayer LCP as the substrate, the antenna array remains compact, light weight, and flexible to reduce the load of the satellite when launched. Figure 63 shows the details of the multilayer stack up from a side view, while Figure 64 shows the corresponding layout of a 4 x 8 element antenna array from a top view. As seen in Figure 63 the probe line layer is connected to the embedded feed line layer through a 10 mil diameter and 5 mil tall via. The signal is then fed to the patches through the slot layer that also acts as a ground plane for the microstrip lines in both the probe line and feed line layers. The patch layer is 10 mil above the slot layer. This separation between the slot and patch has a dominant effect on the bandwidth of the antenna. The square patch sides are 0.48 λ and each patch is separated by 0.52 λ. The reason why the patches are not exactly λ/2 is because of the fringing field effect that increases the effective electrical length of the patch. The 1 mil LCP layers act as bonding layers between the 4 mil and 9 mil core layers. In Figure 64, the antenna structure includes a partially embedded corporate feed network, which includes an area for embedding

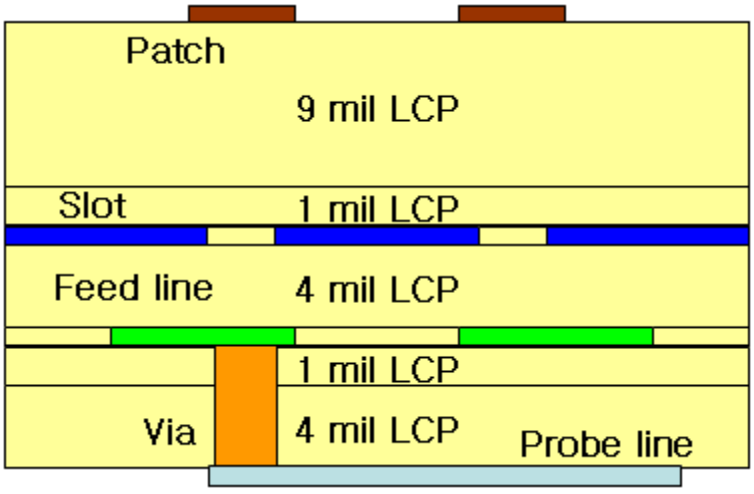



Figure 63: Stack up of the antenna array.

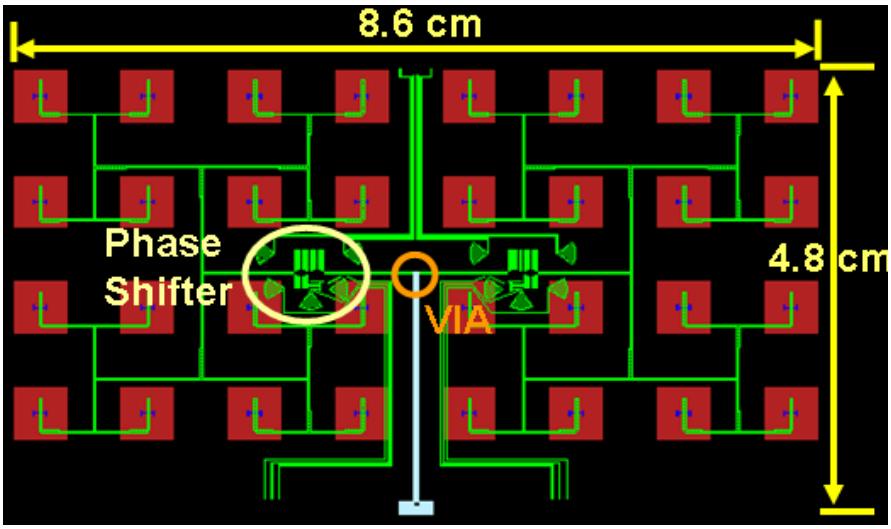



Figure 64: Composite view of 4 x 8 layout.

RF components. In this case, a hardwired, or fixed phase, 2-bit phase shifter is included in the feed line layer. This is a preliminary design for MEMS enabled phase shifters that include the bias lines routed to the edges. Each 4 x 4 unit array includes a single 2 bit phase shifter. The overall size of the 4 x 8 antenna array is 8.6 cm by 4.8 cm.

Figure 65 shows the measured S11 response of the 4 x 8 antenna array with no phase shift. The sharp resonance shows the operating frequency of the antenna array. The other line shows the response when a metal plate is set in the vicinity of the patches, thus, reflecting all radiated power. The result shows that the steep resonance disappears with the metal plate near the radiating elements, which verifies that the antenna array is working properly at 13.8 GHz. The remaining dips in the response do not disappear with the placement of the metal plate, which means that they are resonances derived from the parasitic inductance and capacitances. Figure 66 shows the simulated $S_{11}$ response of the 4 x 8 antenna array with the feed line layer on a single layer as well as split onto multilayer. The single layer response is when the input of the feed is all on the feed line layer. The multilayer response has the input on the probe line layer and the feed uses a

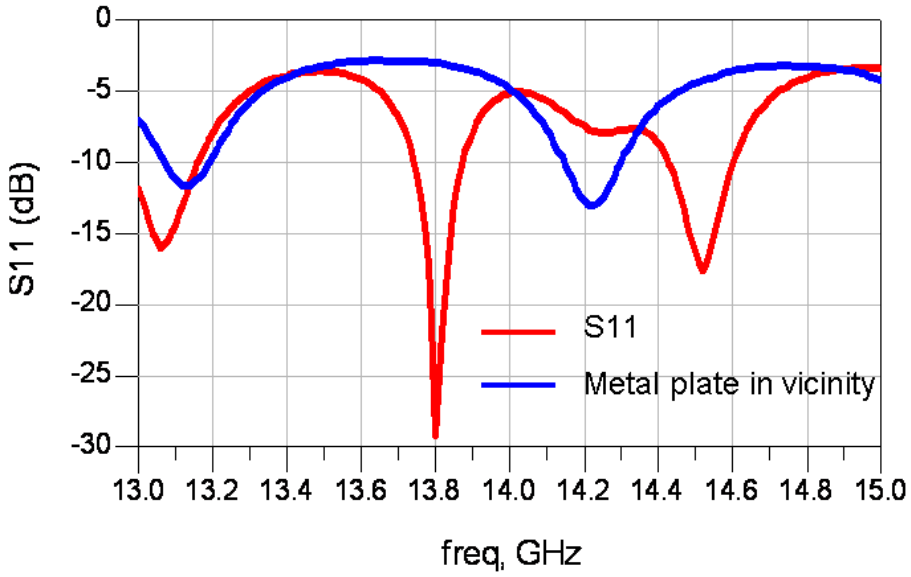



Figure 65: Return loss measurement of the 4 x 8 antenna array with no phase difference.

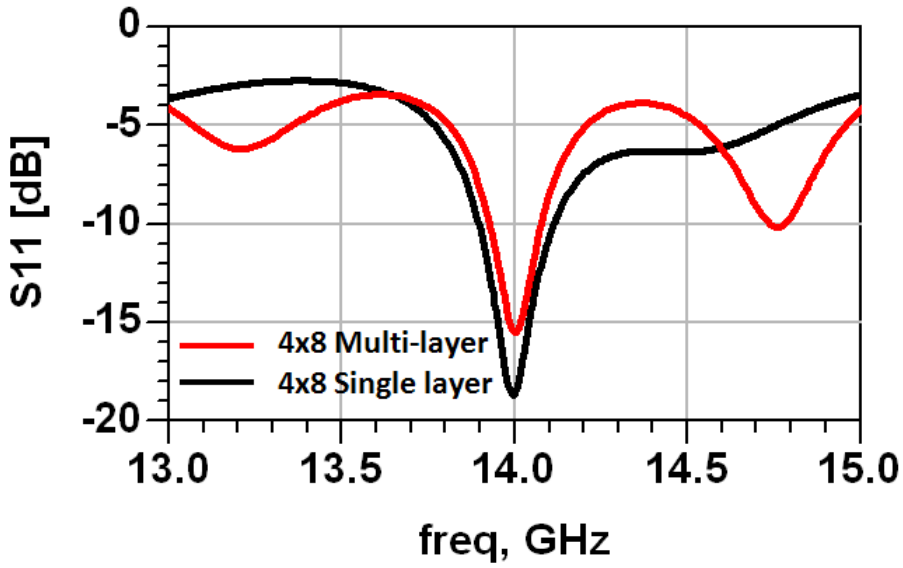



Figure 66: Simulated comparison of the reflection coefficient of multilayer feed and single layer feed with no phase shifter.

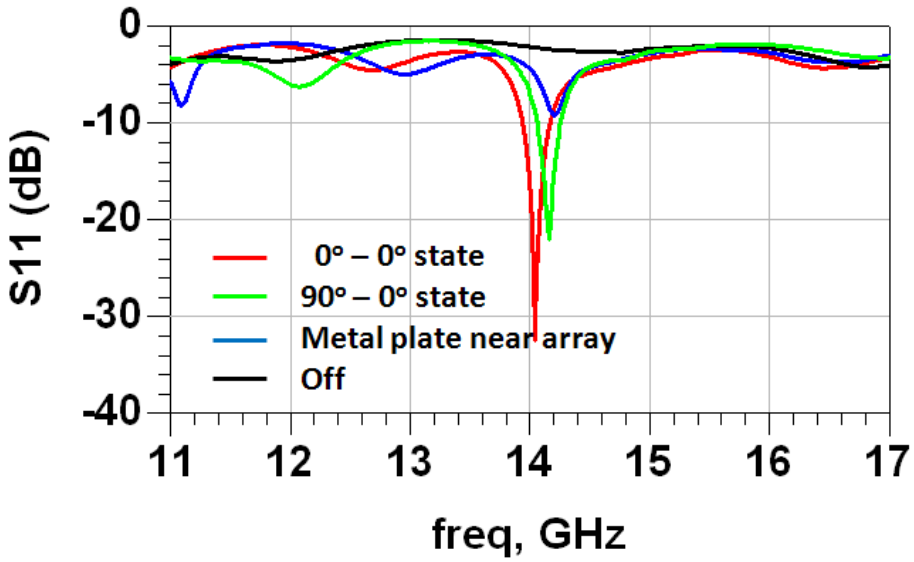



Figure 67: Measured reflection coefficient of RF MEMS switch enabled 4 x 8 antenna array.

via to access the feed line layer. The via introduces extra parasitic capacitance and inductance to create non-radiating resonances in the feed line. Figure 67 shows the measured $S_{11}$ response of a 4 x 8 phased antenna array with actual RF MEMS switches. Though the resonances are slightly apart, the $0^o$ – $0^o$ state and $90^o$ – $0^o$ state clearly show a radiating resonance while the off state isolates the signal to the radiating elements. Figure 68 shows the measurement of the 4 x 8 phased antenna array with the biasing of the MEMS switches. A thick Styrofoam block is placed underneath the antenna array to separate the metal sample holding chuck from the radiating patches that are on the other side of the feed lines.

Figure 69 shows the measured antenna pattern of a 4 x 8 element antenna array with the two phase shifters in three different states. The first state is in which both phase shifters have the same phase shift of $0^o$ shown as the middle pattern of the three. The resulting pattern shows a 3-dB beamwidth of $12^o$ in the *H*-plane and approximately $24^o$ in the *E*-plane. The measured gain is 15.4 dBi with a SLL (Side Lobe Level) 13 dB below the maximum.

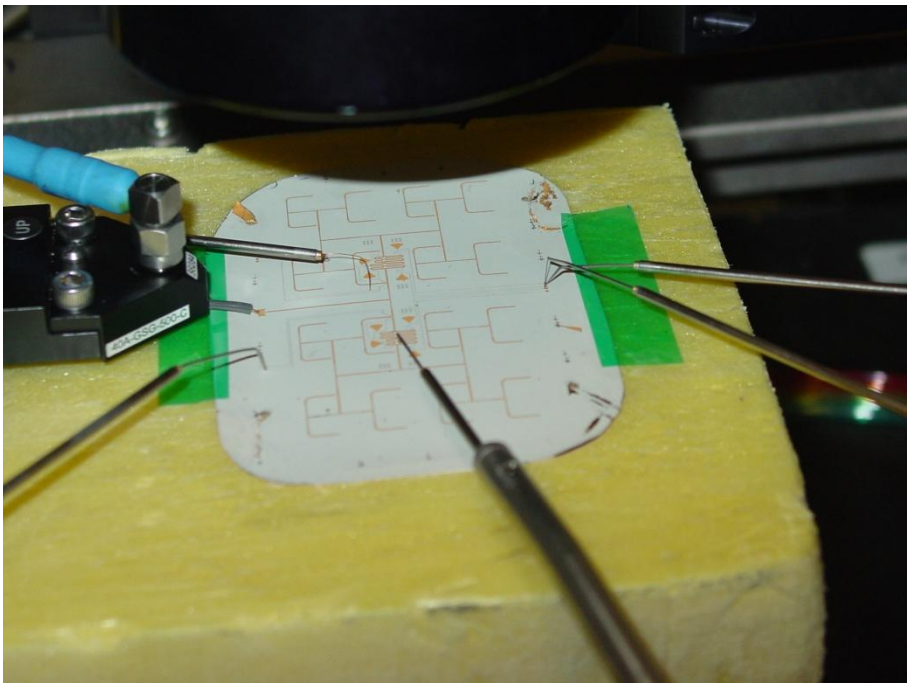


Figure 68: Measurement setup for 4 x 8 antenna array.

Using equation (2), we can calculate the directivity of the 4 x 8 antenna array to be 20.04 dBi. In an ideal case with the radiation efficiency of 1, the maximum directivity is equal to the gain of the antenna. Thus, assuming ideal aperture efficiency of 1, the 4 x 8 antenna array with 32 patch elements should have a gain of 20.36 dBi. The measured gain is approximately 5 dBi lower than the ideal gain because of the line loss from the feeding network and possible leakage in the slot coupled feed of the patches. A rough estimate can be made to verify the loss that has been measured. The microstrip line length from the feed point to the antenna is approximately 9.5 cm. With a line loss of 0.25 dB/cm on LCP [59], about 2.37 dB is contributed to the line loss. The meander lines in the phase shifter roughly add 0.2 dB of loss. In addition, with slight fabrication errors, each T-junction adds about 0.3 dB of loss contributing to an additional 1.5 dB loss. The simulated via adds an additional 0.4 dB of loss as a square patch twice the size of the via is added as a landing pad. Thus, including the error factor, the total loss is 4.97 dB, which

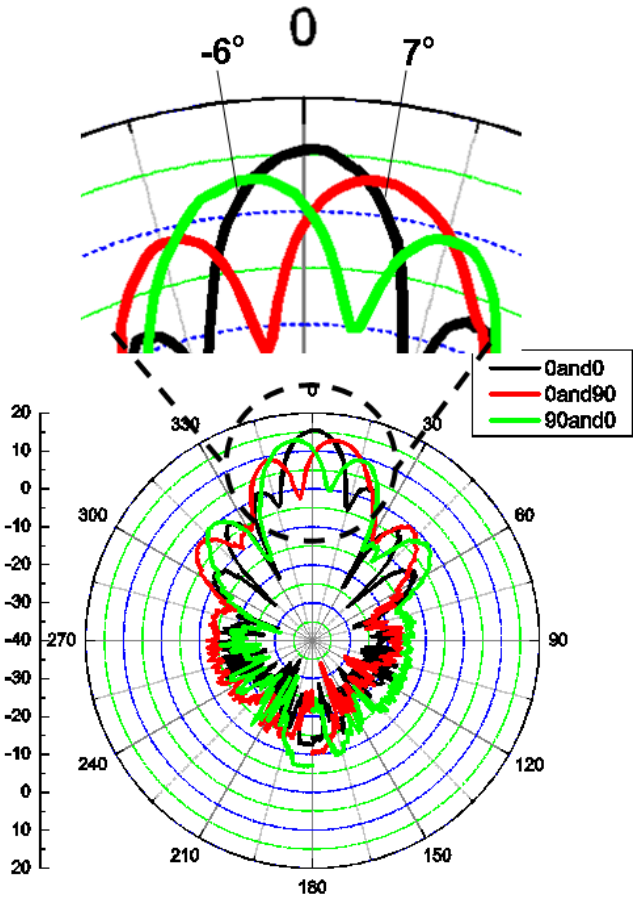
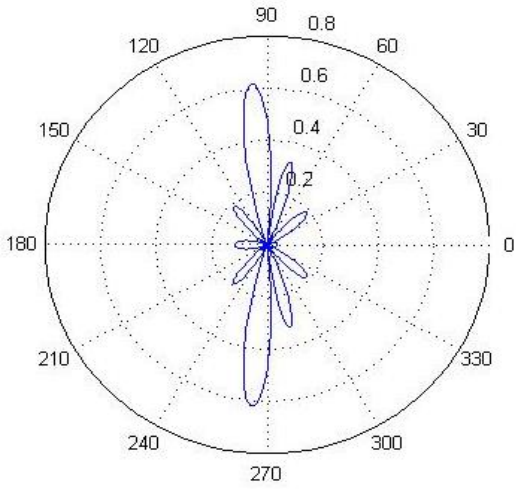



Figure 69: 4 x 8 antenna pattern measurement of the $H_{co}$ field with and without $90^{o}$ phase shift.

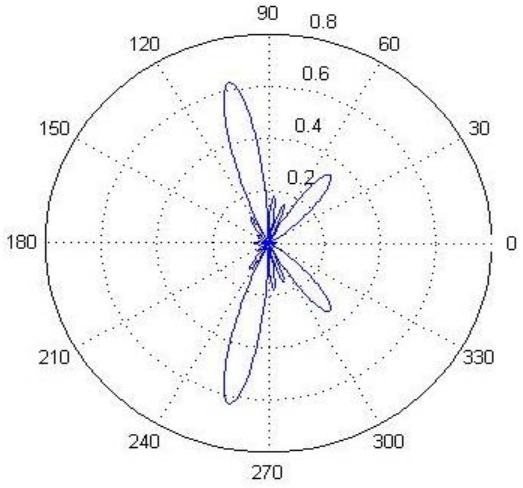
is close to the calculated ideal gain. In addition to these estimated numbers, additional loss can be attributed to leakage from the coupling slots.

When a $90^{o}$ phase shift is applied to either side of the 4 x 8 array, the resulting beam steers approximately $6.5^{o}$ away from the maximum, also seen in Figure 69. The gain drops to 13 dB and the SLL rises to only 4.2 dB lower than the main lobe, almost splitting the main beam. This can be avoided if the phase shift is applied to a smaller unit array such as a 2 x 2 or ideally every element, which will also increase the maximum beam steer angle. Figure 70 shows a simulated radiation pattern of a linear 8 element phased antenna array with $90^{o}$ phase increments given to a group of radiating elements.

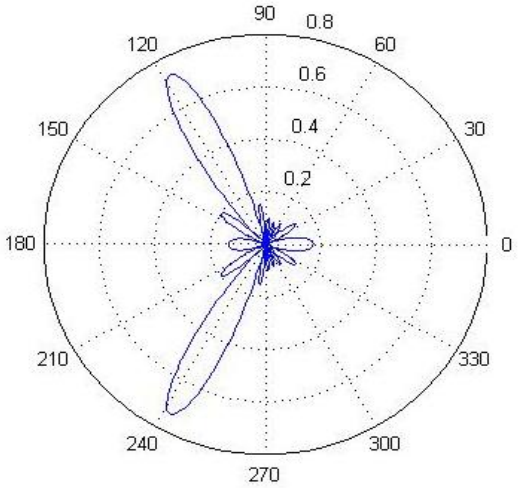
Figure 70 (a) divides the 8 elements into two groups of four and applies a $90^o$ phase difference between the two. A maximum of $7.5^o$ beam steer is achieved in this configuration. When the 8 elements are divided into four groups of two, as Figure 70 (b), a maximum beam steer of $15^o$ is accomplished. Finally, as shown in Figure 69 (c), a maximum beam steer of $30^o$ is ideally achieved with $90^o$ phase increments between every element. In the case of the 4 x 8 phased antenna array, the two phase shifters are used in the 8 element direction giving the same phase to two 4 x 4 element arrays. This is equal to the antenna pattern in Figure 70 (a). Thus, to reduce the side lobe levels of the steered beam, additional phase shifters are needed that will also allow to achieve a larger maximum beam steer.




(a)




(b)




(c)

Figure 70: Simulated 8 element antenna array pattern with a phase shifter for every (a) 4 elements, (b) 2 elements, and (c) 1 element.

## 6.3 8 x 8 Antenna Array

The 8 x 8 antenna array is twice the size of the 4 x 8 antenna array at 8.6 cm by 8.7 cm, as shown in Figure 71. The size is larger than a 4 inch circle, which is the desired processing limit. It is possible to process bigger sample sizes, but at the cost of yield and non-uniformity across the sample. Also, the guaranteed minimum feature size becomes larger than desired with larger samples, and again, it may not be uniform. In addition, this is a representation of creating an antenna array beyond the fabrication capabilities. In order to avoid these fabrication complications, a 4 x 8 antenna array is the unit array and "stitched" to create a larger 8 x 8 antenna array. The via transitions are used to connect the probe line on the bottom to the embedded feed line.

The antenna design is based on the 4 x 8 sub-arrays presented in Chapter 6.2. Two sub-arrays are connected using vias on the probe line layer, which is termed

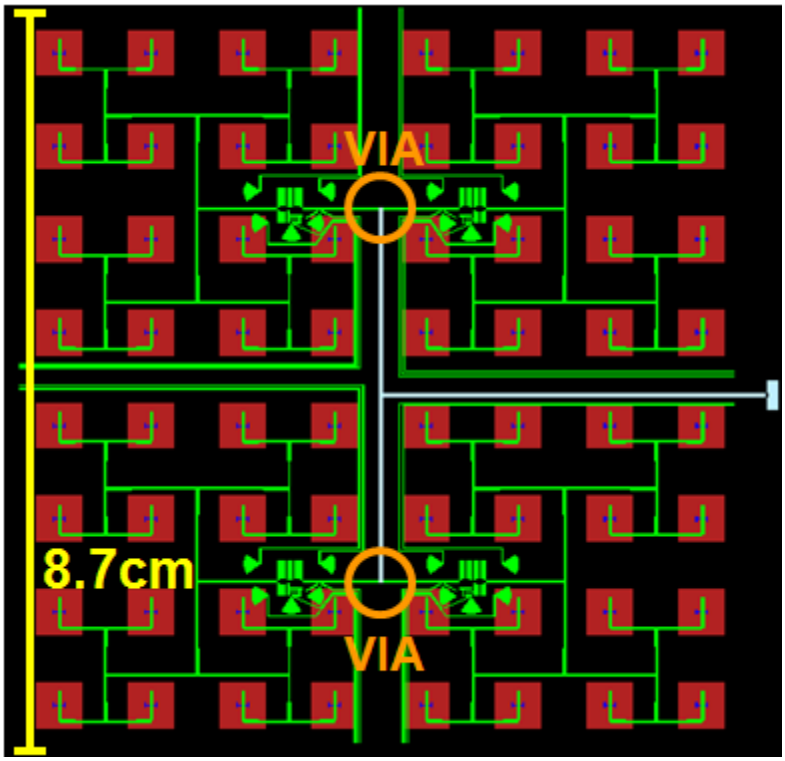
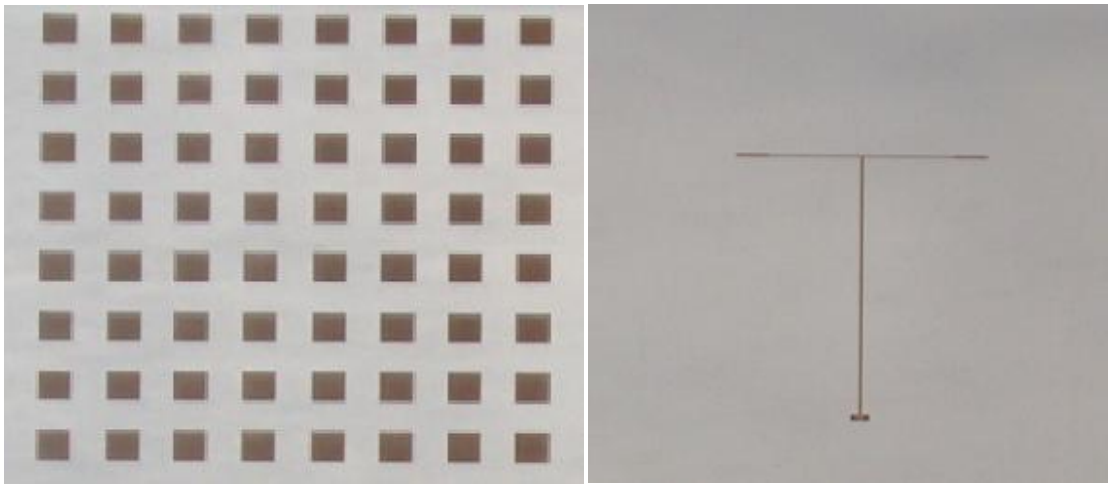



Figure 71: Layout of 8 x 8 antenna array.



(a) (b)

Figure 72: Fabricated 8 x 8 antenna array (a) patch layer (b) bottom feed layer.

as ‘stitching’ a layer. The antennas are fabricated using multi-layer LCP processing technology with laser ablated and electroplated vias to accomplish vertical interconnections. The fabricated sample is shown in Figure 72. Figure 72 (a) shows the patch layer while Figure 72 (b) shows the probe line layer. The rest of the feed lines and slots in the ground are embedded.

Figure 73 shows the measured $S_{11}$ response of the 8 x 8 antenna array. The resonant frequency is at 13.8 GHz, where the fabrication tolerances have affected the operating frequency to shift. Again, a metal plate is placed in the vicinity of the radiating elements to ensure that the patches are radiating. The resonance at 13.8 GHz disappears with the placement of the metal plates, which confirms the radiation. The other resonances at 13.1 and 14.5 GHz remain but shifted. These resonances are internal to the feed line structure that incorporates via transitions. The measured antenna pattern is shown in Figure 74 with a 16.9 dB of gain and a SLL 9.3 dB below the maximum. The calculated ideal gain using equation (16) is 23.4 dB, which is 6.5 dB more than the measured gain. Again, the main source of the loss is the long corporate feed network. The signal path is approximately 14 cm that accounts for 3.5 dB of loss. The remaining 3 dB

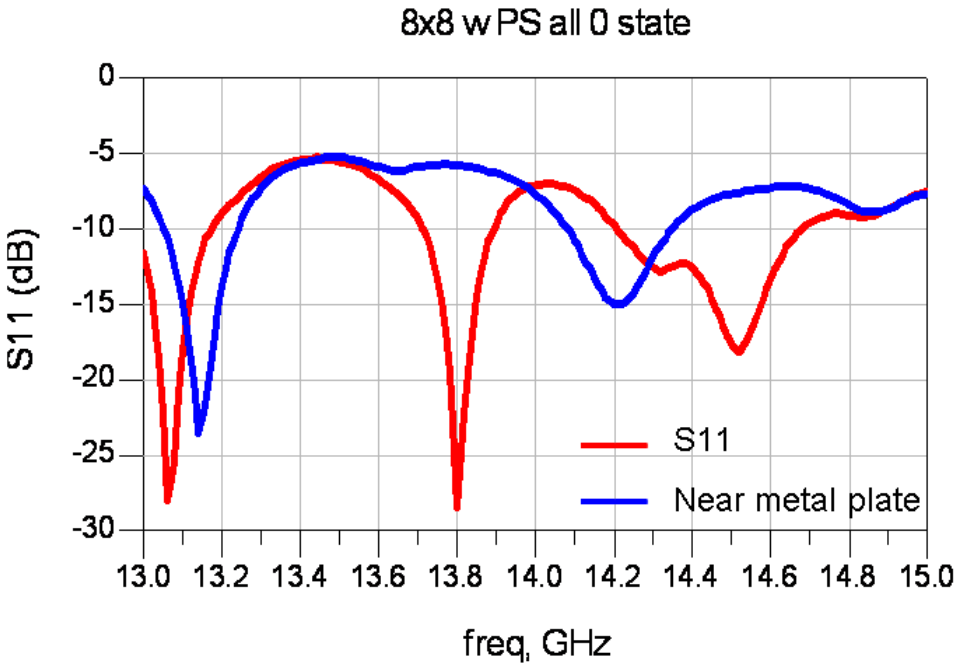



Figure 73: Measured reflection coefficient of 8 x 8 antenna array.

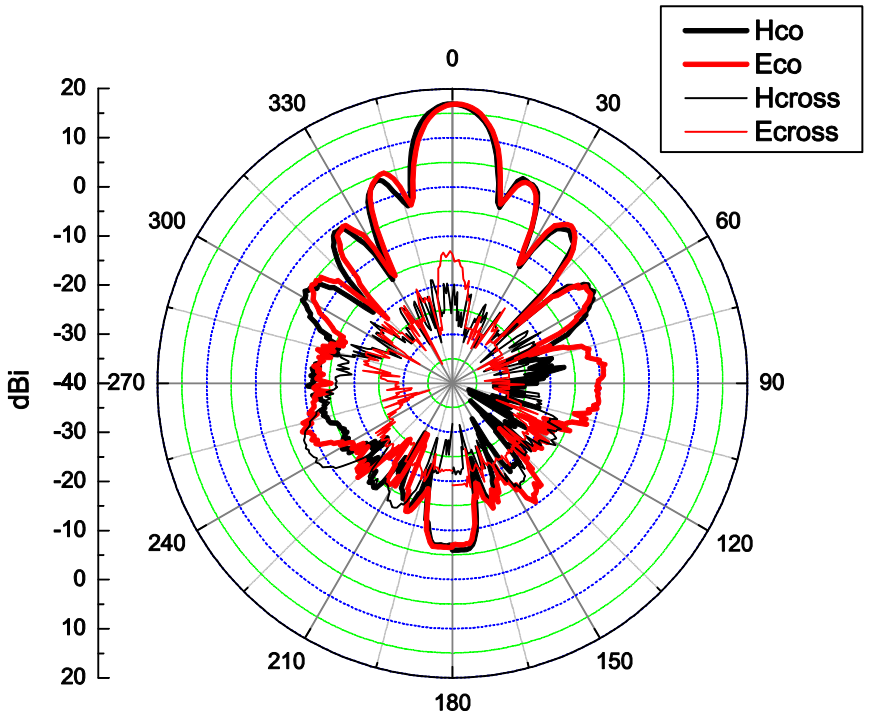



Figure 74: 8 x 8 antenna array pattern measurements.

of loss is attributed to the mismatch arising from fabrication tolerances, small losses in the T-junctions, and possible radiation from the slots. In addition, the vias and the landing pads are sources for the loss as well. The 3-dB beamwidth is approximately $13^{o}$ in both the $E_{co}$ and $H_{co}$ planes, which is consistent with the 4 x 8 element array.

Next, the 8 x 8 antenna is mounted on a cylindrical Styrofoam with a radius of 6.5 cm as shown in Figure 75. Two measurements are made with the antenna array on the Styrofoam; one having the patches facing the center of the cylinder and the other with the patches facing outward away from the center of the cylinder. The measured patterns are shown in Figure 76 and Figure 77. The $H_{co}$ patterns in both cases show a broadened pattern with degradation in the gain and the maximum approximately $50^{o}$ away from the broadside. Similar results and solutions to correct these effects of conformed antennas have been reported [80], [81]. The results show that the antenna array operates correctly while being flexed and can be designed as a conformal antenna.

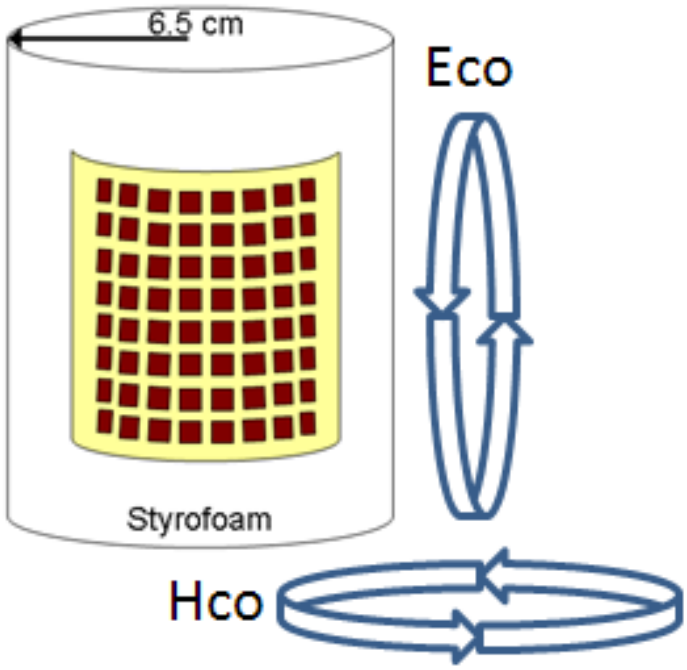



Figure 75: 8 x 8 antenna array on a 6.5 cm radius curvature.

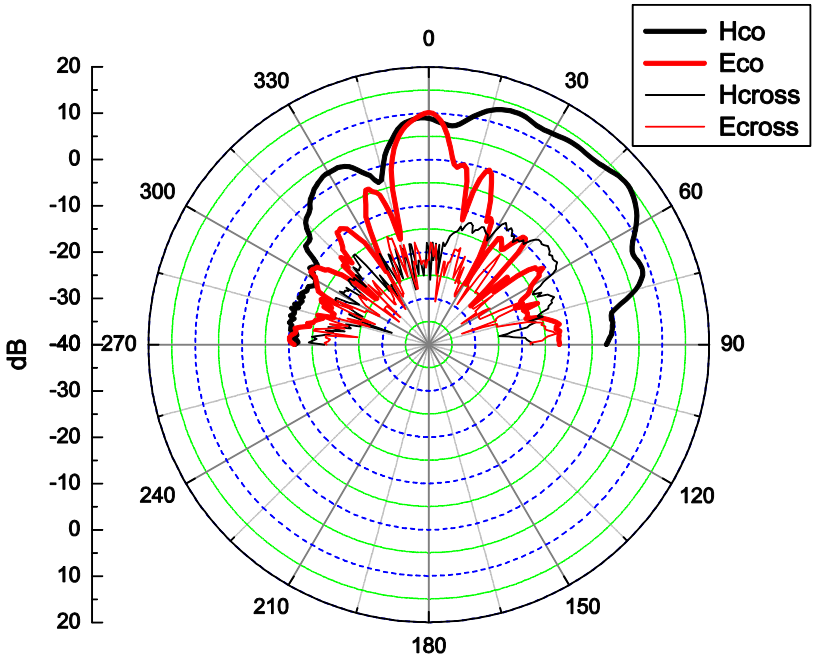



Figure 76: Pattern measurements of antenna on a 6.5 cm radius curvature with the patches facing inward.

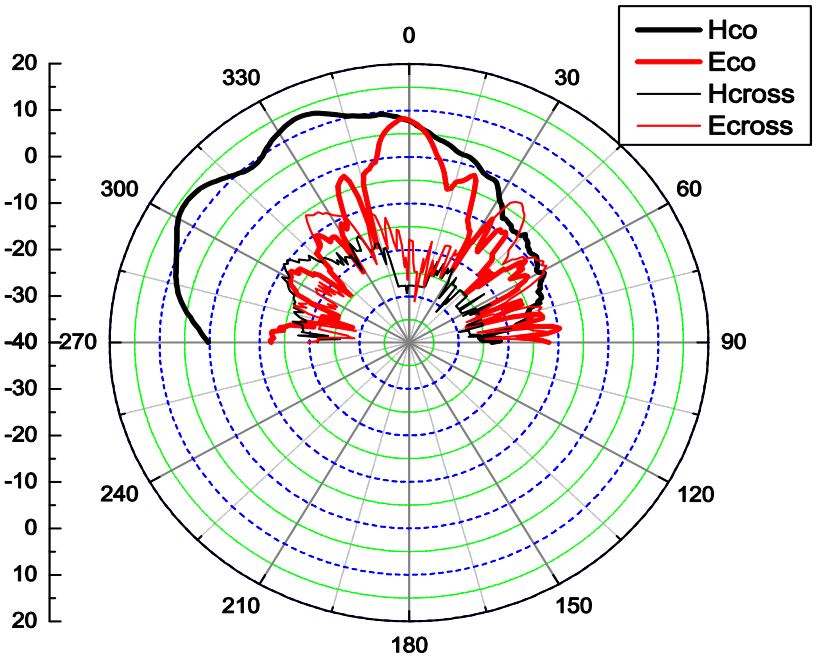



Figure 77: Pattern measurements of antenna on a 6.5 cm radius curvature with the patches facing outward.

## 6.4 16 x 16 Antenna Array

Figure 78 shows the layout of the 16 x 16 element antenna array design. As a preliminary version of a MEMS phased array, the hardwired phase shifters are included with long bias lines routed to the edges of the antenna. The overall size is 18 cm by 18 cm. Even with a thickness of 19 mils, the antenna array maintains its flexibility and light weight. The 256 element array is based on 'stitching' eight 4 x 8 arrays that are presented in Chapter 6.2 and the stack up of the layers is the same as Figure 63.

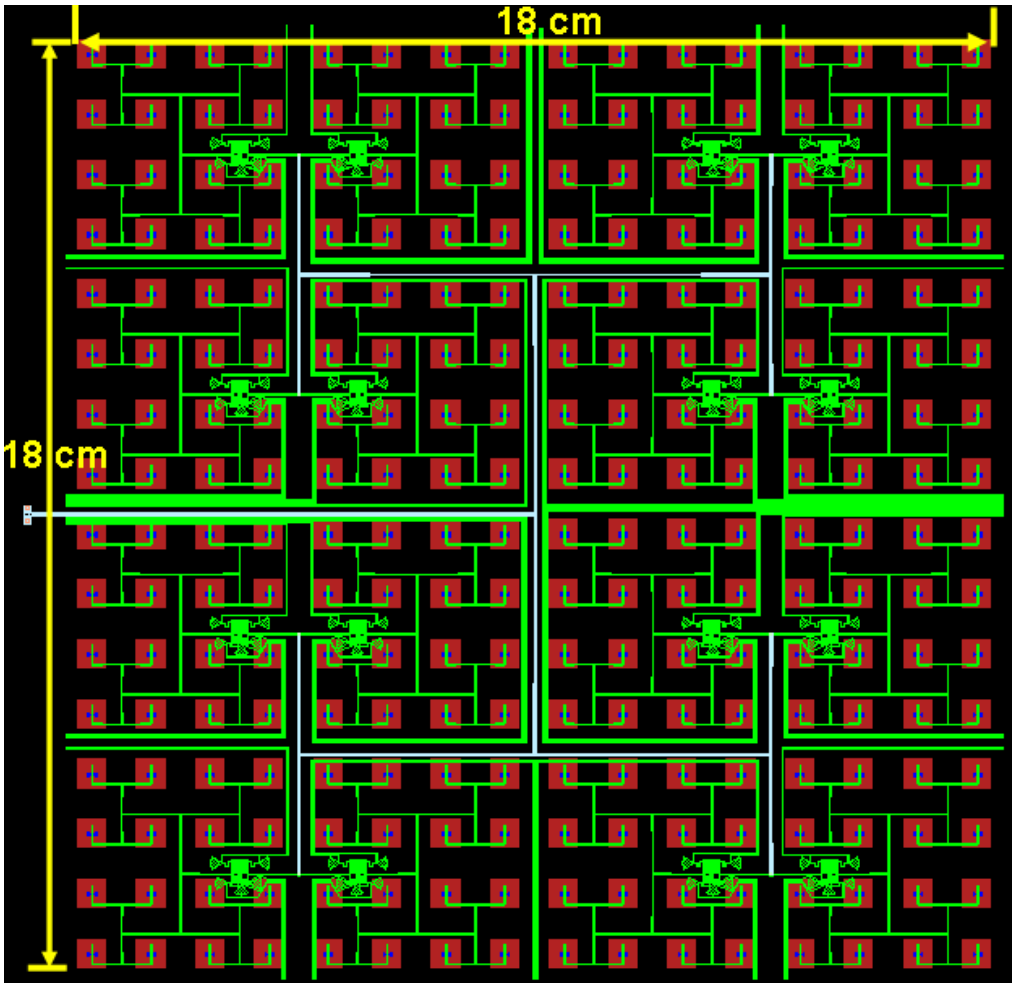



Figure 78: Layout of a 16 x 16 antenna array with hardwired phase shifters and bias lines.

Figure 79 shows the antenna pattern measurement set up and Figure 80 shows the resulting antenna pattern measurement of the 16 x 16 antenna array. The 3-dB beam width, in both the *E*- and *H*-plane, is measured to be $6^{o}$ and the SLL is approximately 9 dB below the main beam. The calculated directivity is 30.04 dB, which is similar to the estimated ideal case. The measured gain is 16.85 dBi, which is relatively low compared to the calculated ideal gain of 29.29 dBi using equation (3). The loss of 12.54 dB can again roughly be verified by estimated calculations. The total length from the feed point to the antenna is roughly 29 cm and with 0.25 dB/cm of loss, the total line loss is estimated to 7.25 dB. There are eight T-junctions that amount to 2.4 dB of loss. The phase shifter, via, and error factor roughly adds 1.1 dB of additional loss. The total estimated loss is 10.85 dB, which still is 1.7 dB lower than the ideal case. Other than the antenna efficiency and the loss from the coupled slots, additional loss can be contributed to the more complex feed network compared to the 4 x 8 array. The long bias lines that run in the embedded layer along the bottom probe line layer can also introduce additional loss. To minimize the coupling between layers and lines, the length of the thinner sections (Zo = 70.7 Ω) in the T-junctions have been elongated, which in return becomes more lossy. These values are estimated values to verify the plausibility of the measured gain.

## 6.5 Summary

In this chapter, a corporate feed multilayer phased antenna array is presented on light weight flexible LCP. Starting with a unit 4 x 8 element antenna array, the array is expanded to show an 8 x 8 element antenna array as well as a 16 x 16 element antenna array. As the antenna size increases, the limitation of the corporate feed network is seen as the line loss increases. One phase shifter is used for each 4 x 4 antenna array and a $13^{o}$ beam steer is achieved with the 4 x 8 phased antenna array. In addition, the flexibility of the LCP is shown with the 19 mil stack up to create conformal antennas.

Figure 79: Measurement setup of 16 x 16 antenna array.

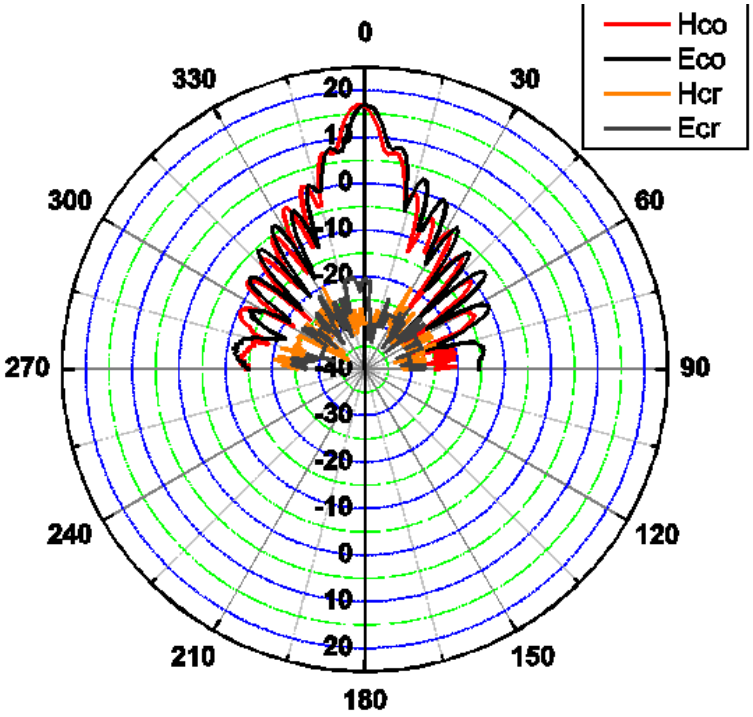



Figure 80: 16 x 16 antenna array pattern measurement.

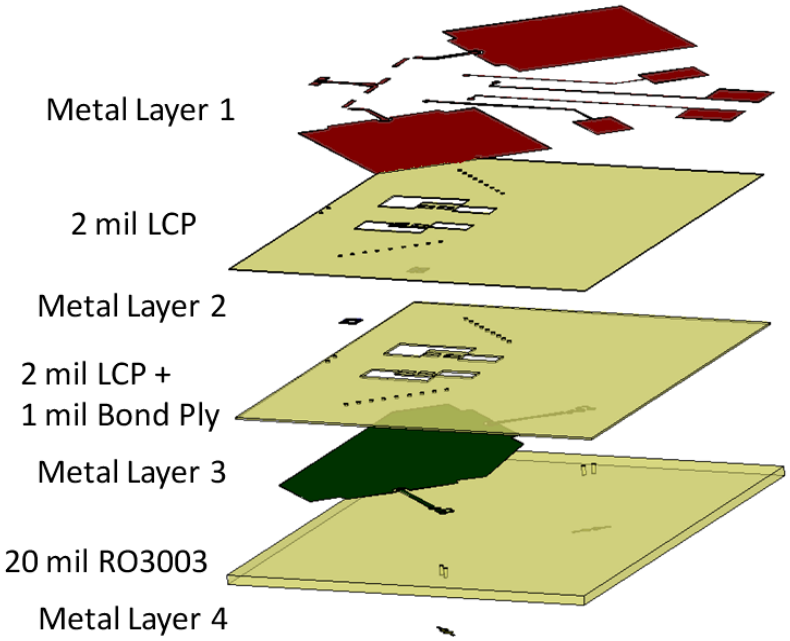
# CHAPTER 7

# 60 GHZ TRANSCEIVER FRONT END

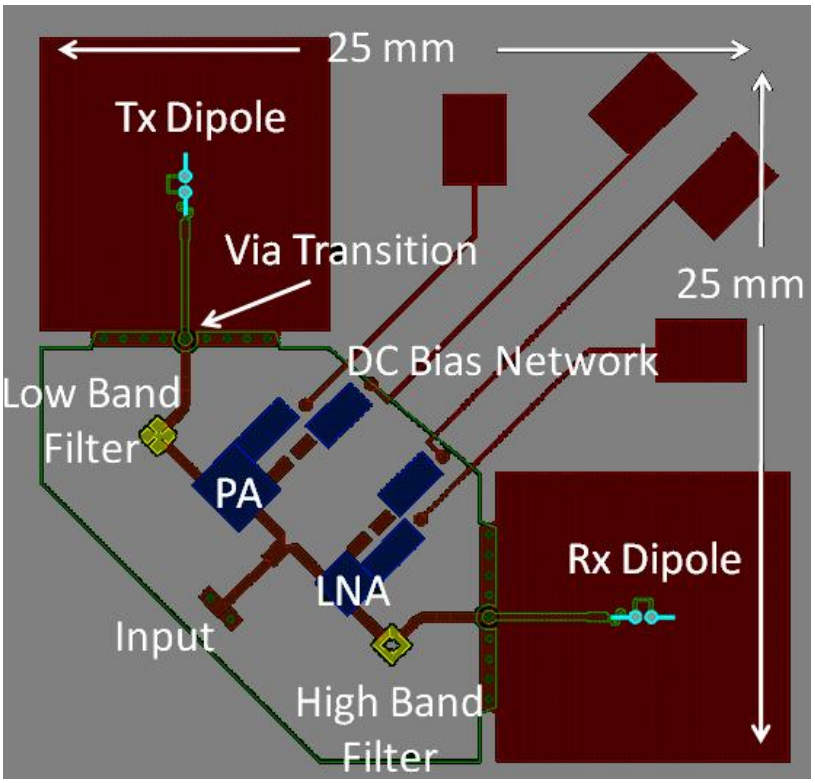
System level integration is particularly challenging at mm-wave frequencies as frequency dependent parasitic effects increase in the devices and interconnects while the overall system is more sensitive to fabrication tolerations. A SOP approach discussed in Chapter 1 minimizes interconnects between components and offers the optimal integration technology. In this chapter, a 60 GHz transceiver front end for simultaneous high speed communication is designed and measured for the first time based on a MLO LCP stack up. This work integrates high gain vertical dipoles and embedded compact dual mode filters with active PA and LNA chips at the packaging level to realize a low cost, lightweight, and highly integrated system for 60 GHz wireless communication applications. Design and fabrication of a device at these frequencies are a particular challenge as frequency dependant parasitic effects from the interconnects and each component have a large affect on the overall performance.

## 7.1 60 GHz Transceiver Layout

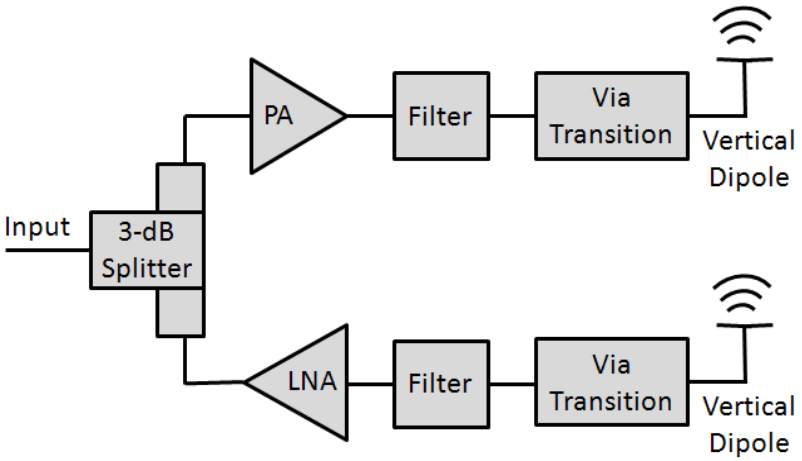
A multilayer design is crucial for creating a compact and efficient design to minimize interconnects as well as isolate sensitive components with an embedded ground. Figure 81 (a) shows the stack up of the proposed design. Figure 81 (b) shows the layout of the transceiver design and Figure 81 (c) is the corresponding block diagram. The CPWG to microstrip transition input followed by a 3 dB splitter is on the top (metal layer 1), 5 mils above the ground plane (metal layer 3). The two filters (metal layer 2) are


Metal Layer 1
2 mil LCP
Metal Layer 2
2 mil LCP +
1 mil Bond Ply
Metal Layer 3
20 mil RO3003
Metal Layer 4

(a)


25 mm
Tx Dipole
Via Transition
25 mm
DC Bias Network
Low Band
Filter
PA
Rx Dipole
LNA
Input
High Band
Filter

(b)




(c)

Figure 81: Multilayer transceiver (a) stack up (b) layout (c) block diagram.

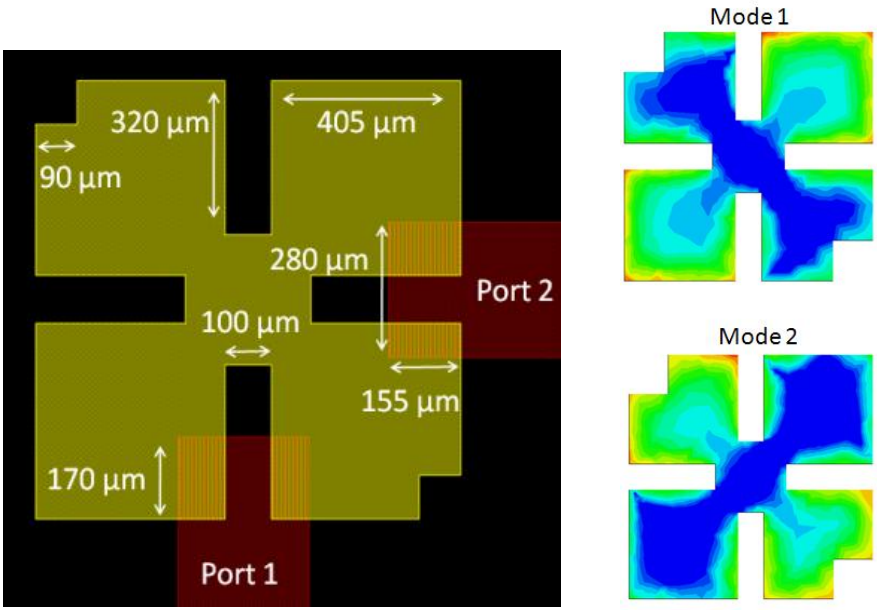
embedded 3 mils above the ground plane. Cavities are drilled using an excimer laser and the active and biasing circuitry components are mounted with conductive silver epoxy. These cavities are essential for high frequency integration to level the active chip surface and the RF lines on the LCP, which result in shorter wire bond lengths. Longer and thinner wire bonds introduce parasitic inductance and resistance that quickly degrades the performance. It is recommended to use 3 mil ribbon bonds with lengths less than 8 mils long. The active chips are connected using 3 mil ribbon bonds while the biasing components are connected with 1 mil wire bonds. The ground plane, which is also embedded, is connected to the top CPW ground using 6 mil diameter vias that acts as both a RF and DC ground. A 5 mil via transition is made from the top metal layer 1 to metal layer 3 connecting to the feed of the vertical dipole antenna. The feed is connected to the dipole antenna (metal layer 4) with 20 mil vias that are placed through the 20 mil thick RO3003 layer. RO3003 is an organic substrate that is compatible with LCP in multilayer stack ups while maintaining similar electrical and mechanical properties to

LCP. Further details of the vertical dipole antenna dimensions can be found in [82].

The operation of the transceiver is based on a duplexer with a 3-dB splitter that divides the two transmitting and receiving modes. The transmitting mode of the duplexer utilizes a Hittite PA that adds 13 dB of gain to the input signal and a band pass filter centered at 59 GHz to cover the lower band of the available 60 GHz spectrum. The PA consumes 400 mW with a 5 V operating voltage. The receiving mode filters the signal from the receive dipole centered at 65 GHz and amplifies the signal by 21 dB using a Hittite LNA. The LNA consumes 160 mW with a 2.5 V operating voltage. The transmitting and receiving dipoles are placed orthogonally to increase the isolation between the modes as dipoles are linearly polarized.

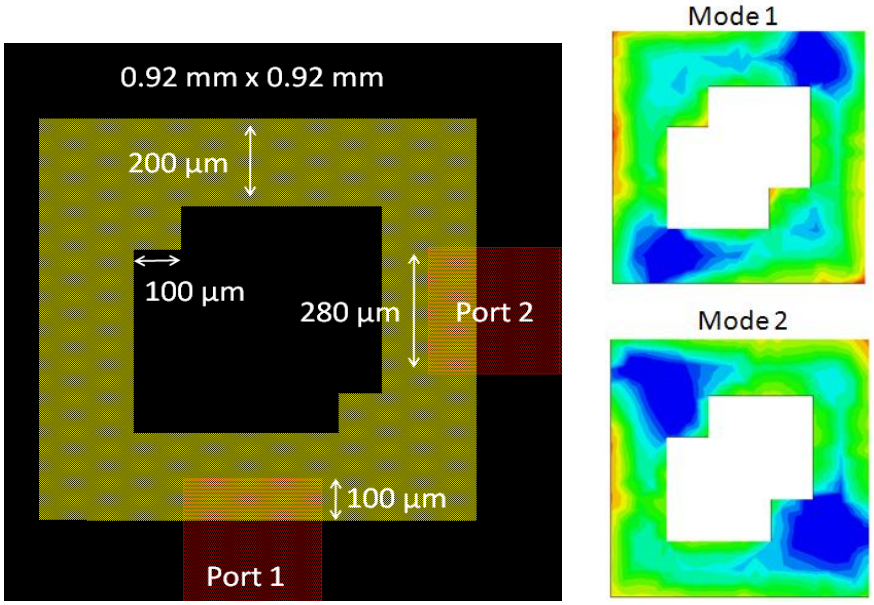
## 7.2 Transceiver Components Design

Dual mode filters have been widely used in wireless communication systems for their compact size and high performance [83], [84]. Two dual mode filters are embedded in the LCP to isolate the transmitting and receiving modes. Ansoft HFSS is used to optimize the dimensions for the lower band and upper band filters that are shown in Figure 82 and 83 respectively along with the two resonant modes. The two filters are planar filters with low Q values due to the thin substrate layer. However, dual mode filters are compact and the planar layout allows easy integration. In addition, the presence of the transmission zeros allow a sharper rejection. The response of the lower band filter, which is a slotted patch filter, is shown in Figure 84 with a transmission zero above the pass band. Figure 85 shows the response of the upper band filter, which uses a $\lambda/2$ ring resonator, with a pair of transmission zero. A higher rejection is achieved with the




(a) (b)

Figure 82: Dimensions of lower band filter (a) layout (b) resonant modes.




(a) (b)

Figure 83: Dimensions of upper band filter (a) layout (b) resonant modes.

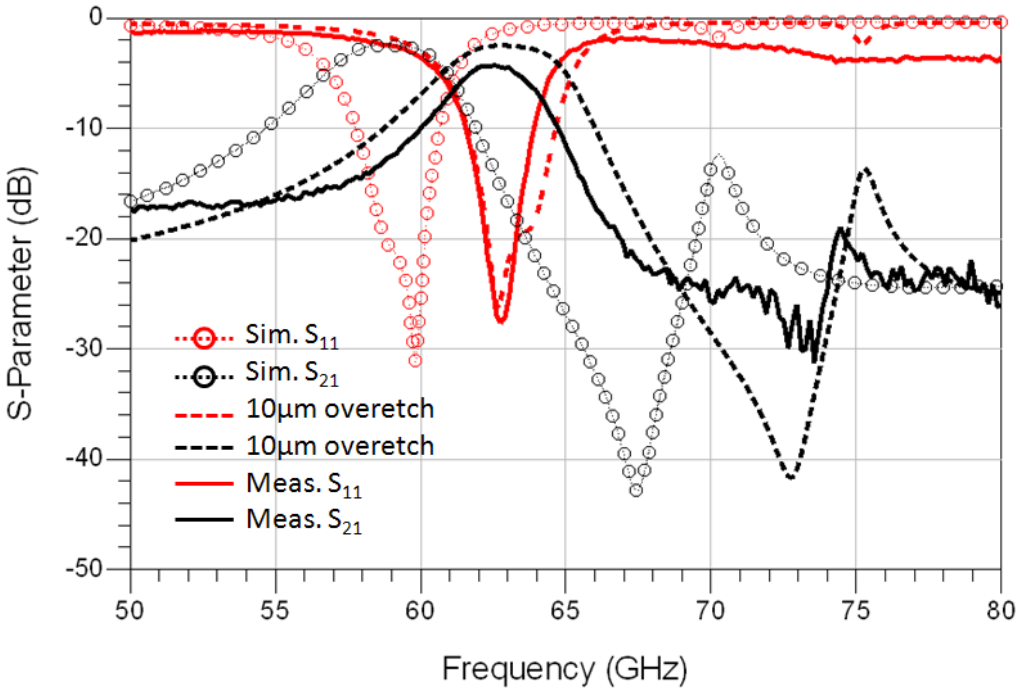



Figure 84: Simulated and measured response of the lower band filter (Figure 81).

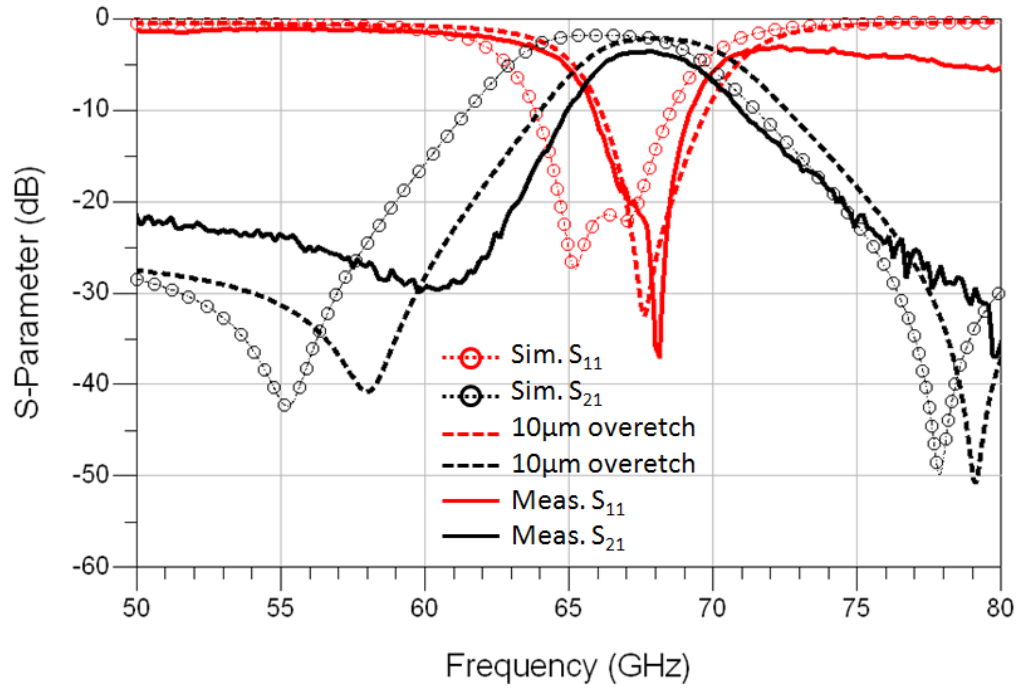
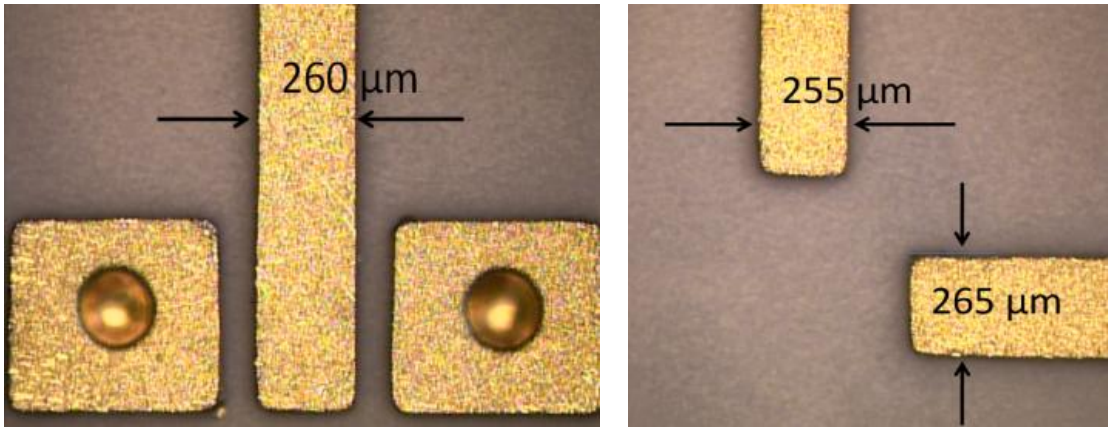



Figure 85: Simulated and measured response of the upper band filter (Figure 82).

transmission zeros, and thus, the isolation between transmit and receive modes is increased. The dual mode resonators are fed by coupling from the input and output ports that are 20 μm offset from the center of the sides. This offset controls the position of the transmission zeros respect to the pass band. The perturbations in both of the filters split the mode of the resonator to create the dual mode response. Larger perturbations increase the coupling between the poles and separate them apart. The slotted patch resonator uses inductive coupling and the ring resonator uses capacitive coupling between the poles. The simulated filter responses were optimized to have an insertion loss of 2.6 dB and 1.8 dB with a center frequency of 59 GHz and 65 GHz respectively, so that the pass bands would cover the upper and lower bands of the 57 GHz to 66 GHz spectrum while maintaining a 15 dB of isolation at 61.5 GHz. After a short, open, load, thru (SOLT) calibration, the measured response for the lower band filter shows an insertion loss of 4.3 dB and a center frequency shift of 3 GHz upward. The upper band filter measures an insertion loss of 3.6 dB and a similar upward frequency shift compared to the simulations. The frequency shift has been found to be due to an over etch in the design as seen in Figure 86. The lines were designed to have a width of 280 μm while the measured line widths at different points of the design are 10 μm over etched on average on each side. The post-simulations with 10 μm over etch included in Figure 84 and Figure 85 verify the frequency shifts in the measurement results. Figure 87 shows a back to back CPWG to microstrip transition with a 2.6 mm microstrip line that can be used to estimate the transition and additional line loss in the filter measurement. The measured transition and line loss are 1.2 dB at 60 GHz so that the insertion loss of the lower band and upper band filters is 3.1 dB and 2.4 dB respectively. The remaining difference can be attributed to the surface roughness. The




(a) (b)

Figure 86: Variations in over etched lines at (a) CPWG input (b) filter feed.

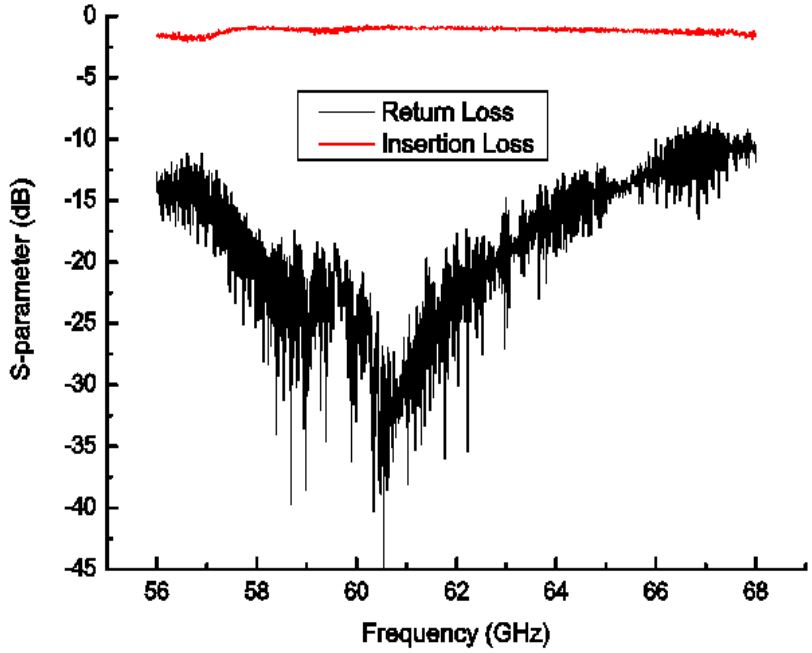
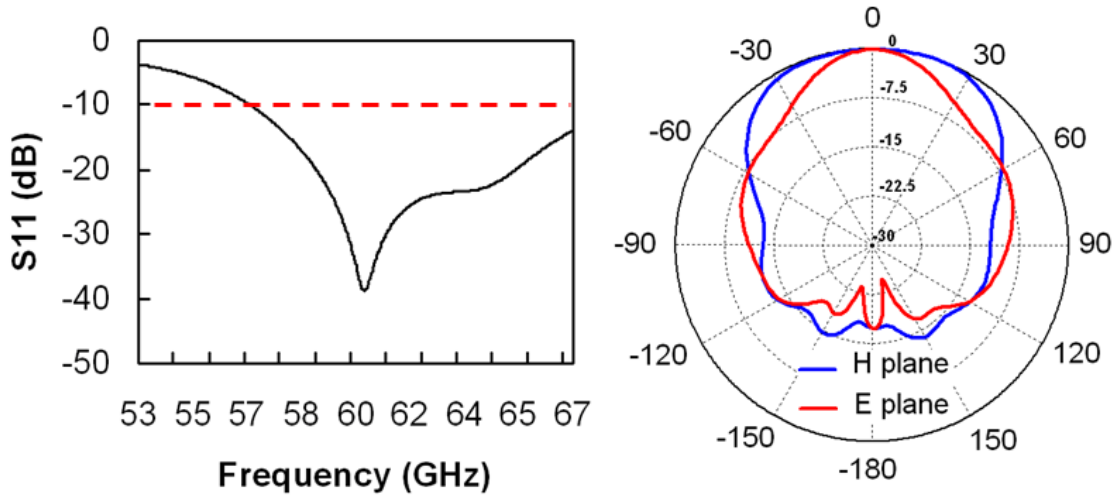



Figure 87: Measured back to back CPWG to microstrip transition with 2.6 mm line length.

measured surface roughness on the Ni/Au plating finish is 0.7 μm and 1 μm on the LCP surface, which are large considering the skin depth at 60 GHz is 0.27 μm.

A wideband package integrated dipole is used for the transmitting and receiving mode antennas. An array of the vertical dipoles has been previously published [81]. Figure 88 (a) shows the simulated return loss of a single dipole that covers the entire 60 GHz band. The normalized radiation pattern is shown in Figure 88 (b) while the dipole antenna is reported to have a gain of 7.65 dBi. The advantages of this vertical dipole are the high gain and integration capability, as it is built with the LCP laminating and metallization process. However, the dipole is sensitive to the size of the ground plane and its surroundings so that the overall system must be included in the simulations for optimal performance.

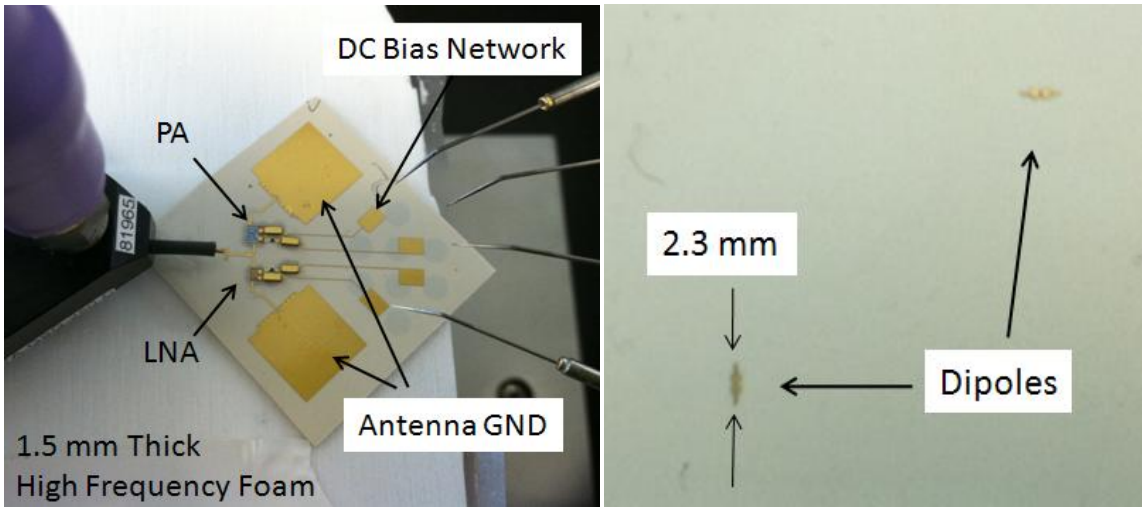



(a) (b)

Figure 88: Simulated (a) $S_{11}$ and (b) radiation pattern of a single dipole.

## 7.3 Integrated System Results

The assembled device is, as shown in Figure 89 (a) and (b), placed on 1.5 mm thick high frequency foam and anchored over a metal chuck for measurement as the radiating element is on the opposite side of the probe input. First, a passive device without the PA and LNA chips is measured to verify the filter and antenna performance. The simulated and measured return loss is shown in Figure 90. Compared to the return loss of a single dipole (see Figure 88 (a)), the responses show a clear rejection in the mid band from the filters. The two resonant points are shifted to 61.5 GHz and 66 GHz compared to the simulated response. Next, the fully integrated transceiver is measured at the two resonant points. The set up of for the radiation pattern measurement is shown in Figure 91 that includes a standard horn and a PNA. The normalized transmitting mode radiation pattern is measured at 61.5 GHz and shown in Figure 92. The normalized




(a) (b)

Figure 89: Test set up of assembled module (a) top (b) bottom.

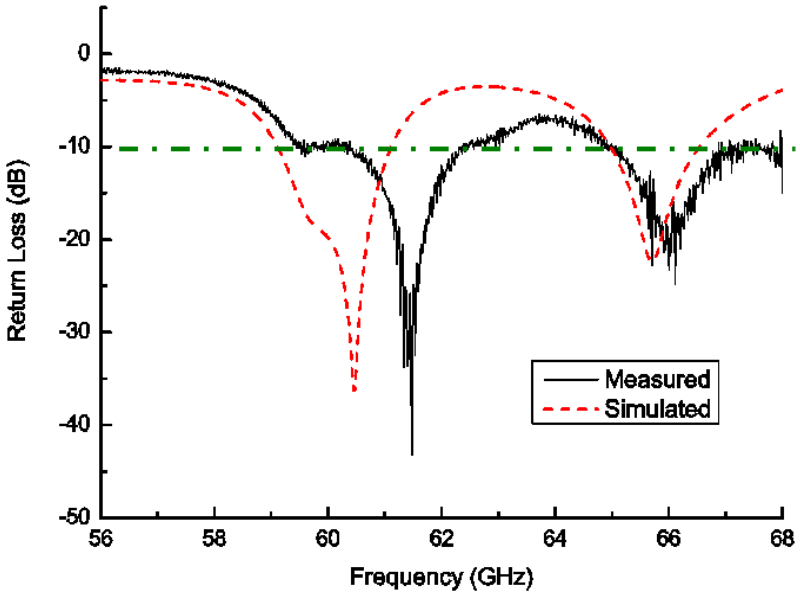



Figure 90: Measured $S_{11}$ response of passive duplexer.

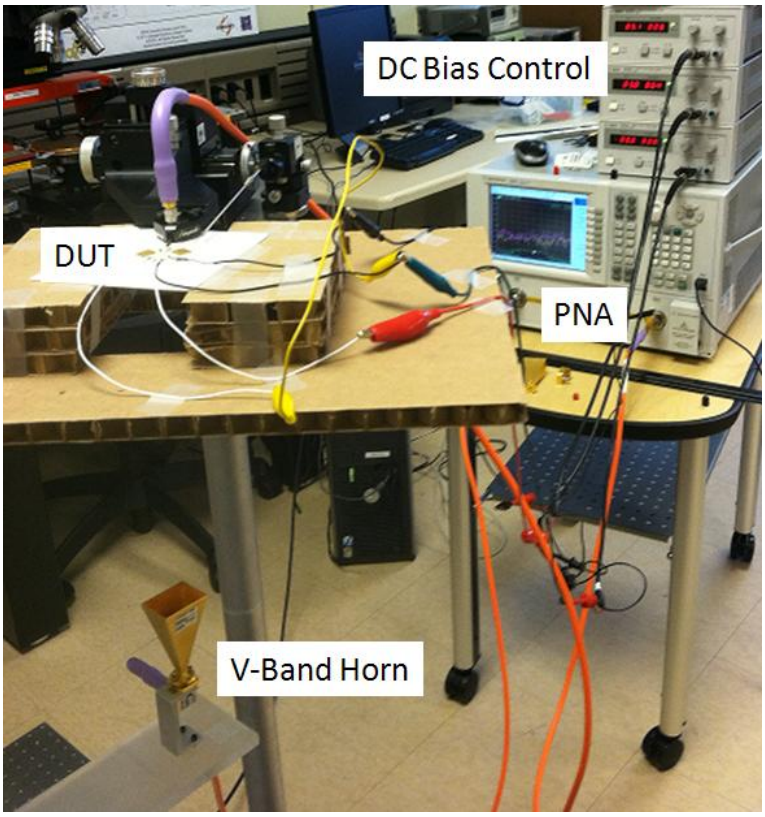
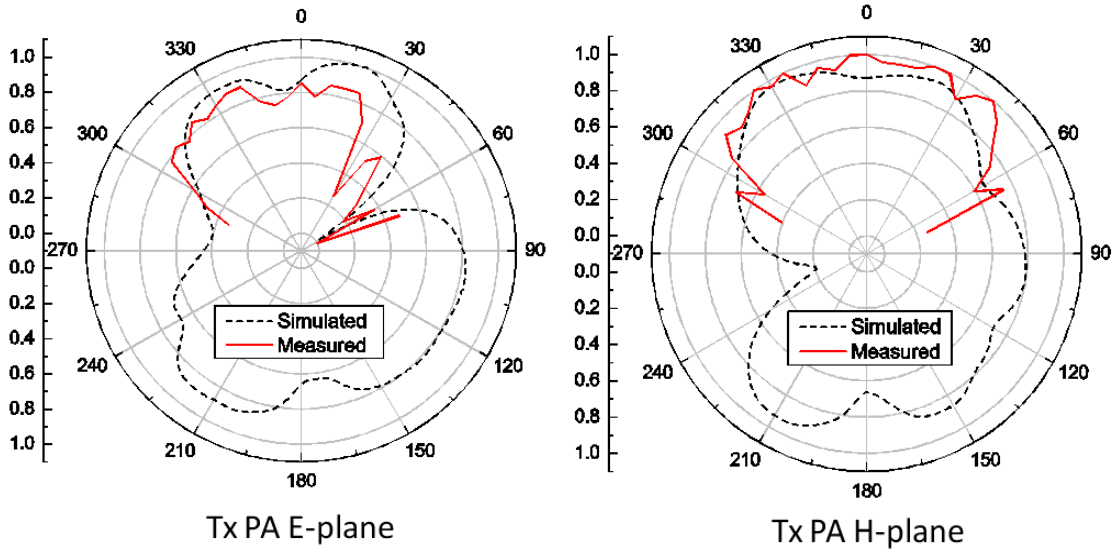



Figure 91: 60 GHz transceiver radiation pattern measurement set up.

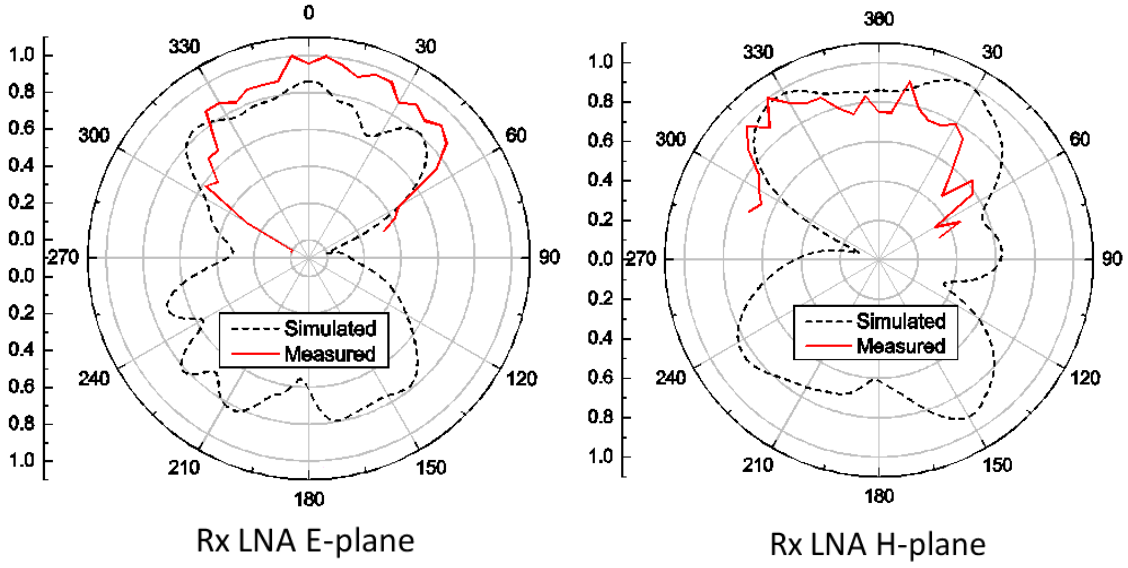
receiving mode radiation pattern is measured at 66 GHz and shown in Figure 93. The measured results agree well with the simulations but compared to the single dipole pattern (see Figure 88 (b)), the patterns are distorted. This is due to having a finite ground plane and added interference from the biasing network. The measurement points are taken every 5 degrees.

The transmitting mode has a measured peak gain of 12 dBi at 61.5 GHz. The PA has a gain of 13 dB and the dipole adds an ideal gain of 7.65 dB. The major sources of loss are 3 dB of loss from the 3-dB splitter and 3.7 dB from the filter and a single CPWG to microstrip transition (subtracting half of the loss from Figure 87). The remaining difference of 1.95 dB can be accounted for by the 5 mil via transition and ideal gain assumption from the simulations that do not account for the processing errors and




(a) (b)

Figure 92: Normalized transmit mode radiation pattern measurement at 61.5 GHz (a) *E*-plane (b) *H*-plane.




(a) (b)

Figure 93: Normalized receive mode radiation pattern measurement at 67 GHz (a) *E*-plane (b) *H*-plane.

Styrofoam. The receiving mode has a measured peak gain of 22 dBi at 66 GHz. The LNA has 21 dB of gain with the dipole adding 7.65 dB of ideal gain. Again, the 3-dB splitter and 3 dB of loss from the filter are the main factors of loss while the remaining difference is from the same sources as the transmitting mode. The accuracy of the gain measurements is ± 2 dB as the measurement set up for a probe fed antenna with back side radiation at high frequencies can be challenging. As seen from the setup in Figure 91, the cardboards are in the Line of Sight (LOS) from approximately 30 degrees away from the center axis adding additional path loss to the measurement. Several factors add to the misalignment of the antennas as well. The plexiglass arm that holds the horn antenna is slightly bent due to the weight of the antenna and cables. In addition, as the antenna is 45 degrees off from the input probe, there is an uncertainty of the alignment of dipole and

the horn antenna polarization. This set up was the first 60 GHz pattern measurement in this lab with a probe fed antenna that has a backside radiation. Additional changes and add-ons to the set up will improve the misalignment errors.

A wireless test is performed to measure the isolation between the two modes as well as the effects of the polarization. The $S_{21}$ and $S_{12}$ response of the PNA is used for measurement with the horn antenna on one port and the 60 GHz transceiver module on the other as seen in Figure 91. Figure 94 shows the measured results where the filters allow approximately 20 dB of isolation between the transmitting and receiving modes in-band. The polarization mismatch allows for additional isolation and shows 10 dB of attenuation in-band.

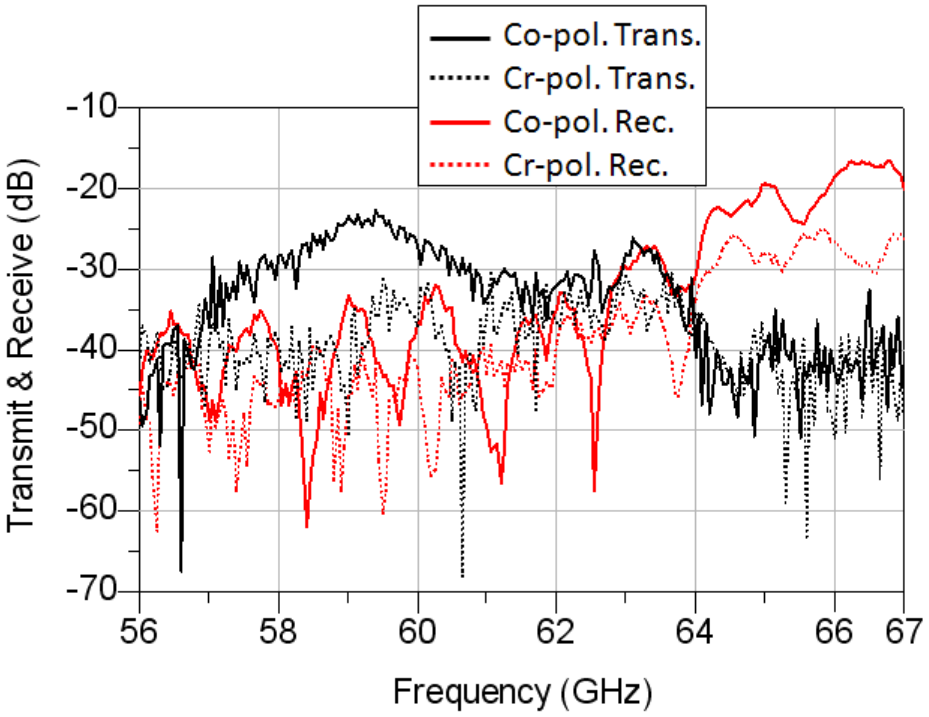



Figure 94: 60 GHz transceiver transmitting mode and receiving mode wireless test.

## 7.3 Summary

In this chapter, a low cost transceiver front end on MLO LCP is presented for 60 GHz wireless communication applications. The multilayer integration of a high gain vertical dipole and embedded dual mode filters at the packaging level show a promising solution for future low cost high frequency wireless communication design. A PA and LNA have been integrated in the design using wire bond interconnects but the possibility of embedding the active components remain for more compact and efficient integration. The final integrated system shows a measured gain of 12 dBi for the transmitting mode at 61.5 GHz and 22 dBi of gain for the receiving mode at 66 GHz. A wireless test is carried out to show the isolation of the transmitting and receiving modes during simultaneous operation.

# CHAPTER 8

# CONCLUSION

In this thesis, LCP has been used to create compact multilayer RF components at a system packaging level. The advantage of using LCP for high frequency RF applications that demand highly integrated and compact systems is clear: low cost, light weight, multilayer processing capabilities, and excellent performance. The work presented in this thesis verifies the above claims by exploring various applications for RF wireless communication.

This thesis explores the enabling technologies and applications for multilayer LCP with a focus on creating compact devices. First, a study on via transitions has been performed as via transitions are essential for multilayer integration. The first low loss HDI transitions on LCP and on LCP/Si hybrid have been designed and measured up to 110 GHz. These transitions allow signals to be routed in varying layers throughout the design with low loss and with minimal space. In addition, the transitions may be used for accessing embedded devices that reduces the interconnect lengths for higher efficiency. Using via technology and LCP/Si hybrid integration, a liquid cooling application is successfully presented with thermal vias in LCP. This is the first active cooling system with organic LCP and silicon. The results show the packaging capabilities of LCP as well as a solution to overcome the integration challenge from the low thermal conductivity of LCP.

Chapter 3, 4, and 5 present RF MEMS switches integrated with RF components on LCP to create reconfigurable and compact devices. RF MEMS switches are monolithically integrated on a multilayer LCP to create a pattern reconfigurable antenna

for MIMO applications. The small size of the RF MEMS and monolithic integration allows the realization of the reconfigurable antenna with minimal interference to the antenna pattern. Using RF MEMS SP4T switches, compact 3D delay line phase shifters are presented. A 3D phase shifter with 85 V electrostatic actuated RF MEMS switches are integrated on a multilayer LCP achieves a 32.4 % overall size reduction. A 2 x 2 element phased array is designed using the phase shifters. Due to the high voltage requirement, the phase shifters have limited integration possibility in a real-world system application. An alternate solution has been presented that uses low voltage PZT RF MEMS switches to create a compact 3D phase shifter. The MEMS switches operate below 10 V and the phase shifter achieves a 22.5 % overall size reduction. This is the first application that integrates PZT MEMS switches on multilayer LCP to create a compact phase shifter.

Next, lightweight antenna arrays are investigated for satellite communication applications. The physical and mechanical properties of LCP provide a compact, conformal, and lightweight antenna array. Starting from a 4 x 8 unit array that includes RF MEMS enabled phase shifter for steering the main beam, a 8 x 8 antenna array and 16 x 16 antenna array have been designed and measured. The multilayer capabilities of LCP allow a compact design where the radiating elements isolated from the rest of the system with an embedded ground. This work has employed a corporate feeding network to systematically expand the antenna array using unit arrays. However, the limitations of the design have been reached as the line loss from the feed network outweighs the gain benefits of the larger array. The 8 x 8 antenna array has been mounted on a conformal

surface and measured to show the flexibility of LCP with promising results for conformal applications.

Finally, a 60 GHz transceiver front end on LCP with simultaneous transmit and receive is presented for the first time. The multilayer stack up allows the integration of embedded dual mode filters and a vertical dipole. Active components such as a PA and an LNA are included with the required biasing network. The measured performance shows a good match with simulations while a high gain is achieved. A low cost solution for 60 GHz wireless communication devices has been shown through the system level integration of the transceiver.

In conclusion, this thesis presents a variety of high frequency applications that take advantage of the use of MLO LCP. Low cost, lightweight, and high performance devices that benefit from the characteristics of LCP have been successfully designed, fabricated, and measured. The results in this thesis show the possibilities of LCP as a future generation high frequency substrate for highly integrated RF systems. Future work remains to overcome the fabrication limitations and integration challenges of LCP to fully develop commercialized low cost RF systems.

# CHAPTER 9

# PUBLICATIONS TO DATE

The following journal and conference papers are listed in chronological order that have been accepted or are presently under review:

## 9.1 Journal Publications

1. **David J. Chung**, Arnaud L. Amadjikpè, and John Papapolymerou, "Multilayer Integration of Low Cost 60 GHz Front End Transceiver on Organic LCP," *Submitted to IEEE Antennas and Wireless Propagation Letters*, Aug. 2011.
2. **David J. Chung**, Ronald G. Polcawich, Daniel C. Judy, Jeffery S. Pulskamp, and John Papapolymerou, "A Reduced Size Low Voltage RF MEMS X-Band Phase Shifter Integrated on Multilayer Organic Package," *Submitted to IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Jul. 2011.
3. Arnaud L. Amadjikpè, **David J. Chung**, Stanis Courrèges, and John Papapolymerou, "A Two-Pole Digitally Tunable Evanescent-Mode Waveguide Narrow Band Filter with RF MEMS Switches," Accepted to *IET Microwaves, Antennas & Propagation*, 2010.
4. **David J. Chung** and John Papapolymerou, "60-110 GHz Low Loss 3D Vertical Transition on LCP packaged Silicon Substrate," *Electronic Letters*, vol 46, issue 8, pg 577 - 578, 2010.
5. **David J. Chung** and John Papapolymerou, "Making the Transition," *Electronic Letters Featured Article*, vol 46, issue 8, pg 546, 2010.

## 9.2 Conference Publications

1. Fan Cai, **David J. Chung**, Evangelos Farantatos, A.P. Sakis Meliopoulos, and John Papapolymerou, "Self- powered Advanced Meter Design Design for Smart Grid," *in Proceedings of Asia-Pacific Microwave Conference*, Dec. 2010.
2. **D. J. Chung**, A. L. Amadjikpe, J. Papapolymerou, "3D Integration of a Band Selective Filter and Antenna for 60 GHz Applications," *in Proceedings of IEEE Antennas and Propagation International Symposium*, Jul. 2010.
3. S. K. Bhattacharya, **D. J. Chung**, Y. Zhang, J. Chen, J. Papapolymerou, "A Hybrid Wafer Level Packaging Technique for Multi-Chip Interconnect Using Low Loss Organic Layers," *in Proceedings of IEEE Conference on Microwaves, Communications, Antennas and Electronic Systems*, Nov. 2009.
4. **D. J. Chung**, S. Bhattacharya, G. E. Ponchak, J. Papapolymerou, "A 'stitched' flexible light weight multilayer 16×16 antenna array on LCP," *European Microwave Conference*, pg. 906 - 909, Oct 2009.
5. **D. J. Chung**, S. Bhattacharya, G. E. Ponchak, J. Papapolymerou, "An 8×8 lightweight flexible multilayer antenna array," *in Proceedings of IEEE Antennas and Propagation International Symposium*, Jun. 2009.
6. **D. J. Chung**, S. K. Bhattacharya, J. Papapolymerou "Low loss multilayer transitions using via technology on LCP from DC to 40 GHz," *59$^{th}$ Electronic Components and Technology Conference*, pg. 2025 - 2029, May 2009.
7. T. Wojtaszek, J. T. Bernhard, G. H. Huff, **D. J. Chung**, and J. Papapolymerou "Reconfigurable Antennas with Integrated RF MEMS Switches for Military MIMO Applications," *Government Microcircuit Applications & Critical Technology Conference*, Mar. 2009.
8. **D. Chung**, S. K. Bhattacharya. J. Papapolymerou, "Phased array antennas on LCP," *Mid Atlantic MEMS Conference*, Laurel, MD, Nov. 2008.

9. Chung-Hao Chen, **D. J. Chung**, S. Bhattacharya, J. Papapolymerou, D. Peroulis, "Low-Cost 3-D Integration of RF and Micro-Cooling Systems," *38th European Microwave Conference*, pg 9 - 12, Oct. 2008.
10. **D. J. Chung**, R. G. Polcawich, D. Judy, J. Pulskamp, J. Papapolymerou, "Low loss piezoelectric SPMT RF MEMS switches," *9th MEMSWAVE Conference*, Jul. 2008
11. J. Papapolymerou, **D. J. Chung**, N. Kingsley, S. K. Bhattacharya, "RF MEMS enabled RF front ends on lightweight organic technology", *9th MEMSWAVE Conference* Workshop on RF MEMS Industry Applications, Heraklion, Greece, Jul. 2008.
12. **D. J. Chung**, R. G. Polcawich, D. Judy, J. Pulskamp, J. Papapolymerou, "A SP2T and a SP4T switch using low loss piezoelectric MEMS," *IEEE MTT-S International Microwave Symposium Digest*, pg. 21 – 24, Jun. 2008.
13. **D. Chung**, S. K. Bhattacharya, J. Papapolymerou, "Development of a Lightweight flexible 16x16 antenna array with RF MEMS phase shifters at 14 GHz," *in Proceedings of NASA ESTC*, Jun. 2008
14. **D. J. Chung**, S. Bhattacharya, G. E. Ponchak, J. Papapolymerou, "A stitching technique for expanding large 3-D multi-layer antenna arrays in Ku-band using small array units," *58th Electronic Components and Technology Conference*, pg. 175 – 178, May 2008.
15. J. Papapolymerou, **D. J. Chung**, N. Kingsley and S. K. Bhattacharya, "Reconfigurable RF front end microsystems," *in Proceedings of 2008 IEEE Conference on Microwaves, Communications, Antennas and Electronic Systems*, Tel Aviv, Israel, May 2008.
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17. **D. J. Chung**, D. Anagnostou, G. Ponchak, M. M. Tentzeris, J. Papapolymerou, "Light Weight MIMO Phased Arrays with Beam Steering Capabilities using RF MEMS," *in Proceedings of IEEE 18th International Symposium on Personal, Indoor and Mobile Radio Communications*, Sept. 2007.
18. Hyungrak Kim, **D. J. Chung**, D. Anagnostou, J. Papapolymerou, "Hardwired Design of Ultra-Wideband Reconfigurable MEMS Antenna," *in Proceedings of IEEE 18th International Symposium on Personal, Indoor and Mobile Radio Communications*, Sept. 2007.
19. **D. J. Chung**, D. E. Anagnostou, G. Ponchak, M. Tentzeris, J. Papapolymerou, "Integration of a 4×8 antenna array with a reconfigurable 2-bit phase shifter using RF MEMS switches on multilayer organic substrates," *IEEE Antennas and Propagation International Symposium*, pg. 93 - 96, Jun. 2007.

# APPENDIX A

# OHMIC RF MEMS SWITCH ON LCP FOR RECONFIGURABLE ANTENNAS

In continuation of the work from Chapter 3.3, where capacitive RF MEMS switches are used, an ohmic RF MEMS switch is designed and fabricated for a reconfigurable antenna in this chapter. The design of a reconfigurable stacked patch antenna has been carried out at the University of Illinois under professor Bernhard and the simulated work has been published [85]. Figure 95 shows half of the top view of the symmetric antenna structure. The S1, S2, and S3 refer to RF MEMS switches. The idea is to use RF MEMS switches to control parasitic elements to achieve a beam steer since the top patch is a parasitic patch. By shorting the MEMS switches in different combinations, a beam steer is achieved as shown in Figure 96. The stack up is shown in Figure 97, where the top patch that includes the MEMS switches on 8 mil LCP has been fabricated at Georgia Tech. The feed is drilled from the bottom and connect to the embedded middle patch. Monolithically integrated RF MEMS switches on LCP are needed for this design as the gap for the switch is only 250 μm. Using IC chips would

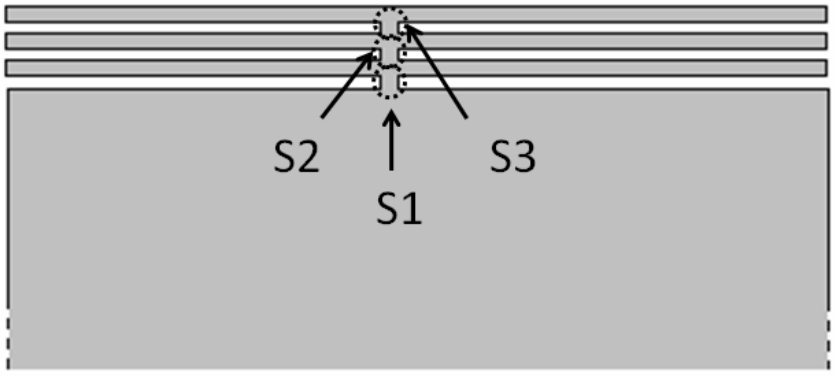



Figure 95: Top view of half of the antenna structure for simulated reconfigurable antenna.

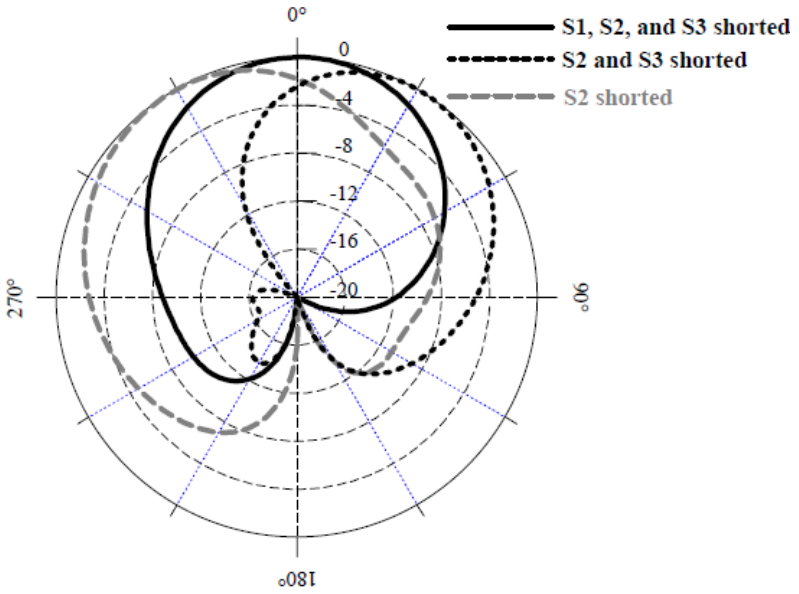



Figure 96: Simulated *E*-plane pattern of the reconfigurable antenna.

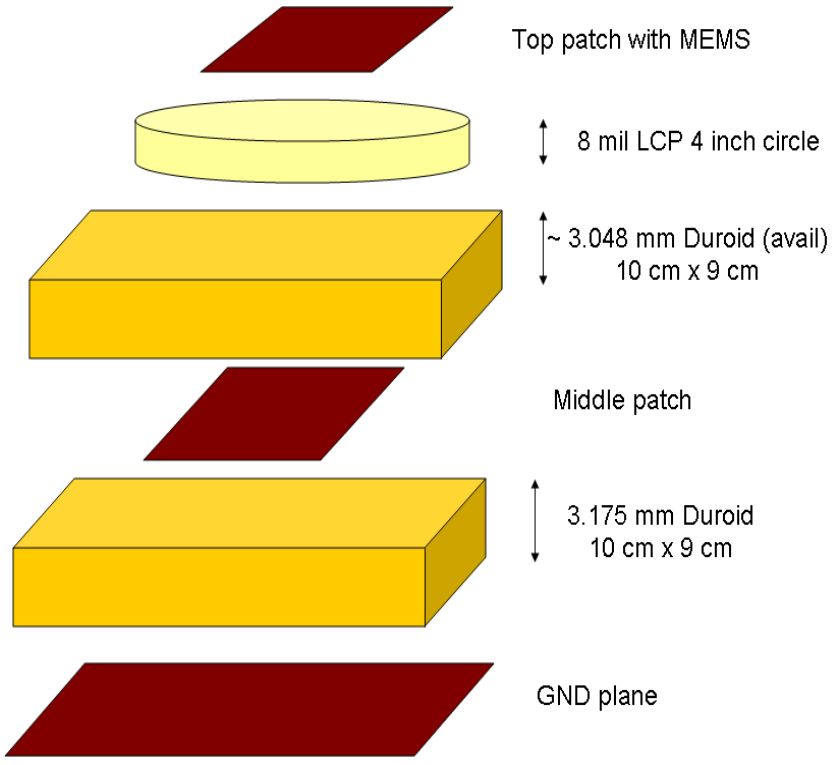



Figure 97: Stack up of the reconfigurable patch antenna.

degrade the performance as the bias circuitry would interfere with the pattern by adding parasitic effects. In addition, the ease of processing multilayer LCP facilitates the fabrication of this design.

Figure 98 shows the final dimensions of the fabricated patch antenna with RF MEMS switches. The fabrication steps are the same as the process described in Chapter 3.2 except for one additional layer in the beginning. The final dimensions including the bias lines are 51 mm by 50.5 mm. Figure 99 shows a view of a single RF MEMS switch. The varying colors on the bias lines are from the varying thickness of the nitride layer on the CrSi. The nitride layer is partially etched in the subsequent steps of the nitride deposition step, but it is sufficiently thick to protect the CrSi layer and not be etched completely. Figure 100 shows a closer view of the RF MEMS switch, and from the focus of the image, it is clear that the membrane is not stuck to the bottom. The individual MEMS switches actuated at 80 – 90 V.

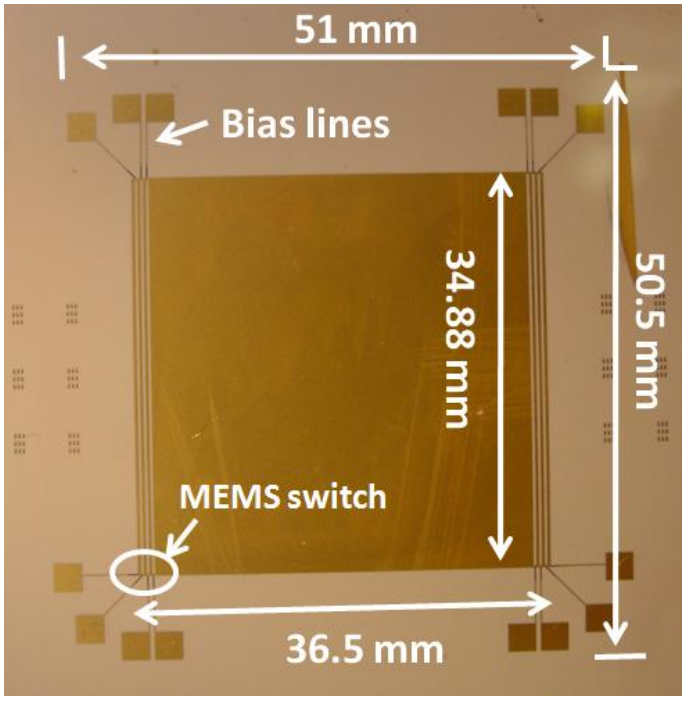



Figure 98: Fabricated patch antenna with RF MEMS switches.

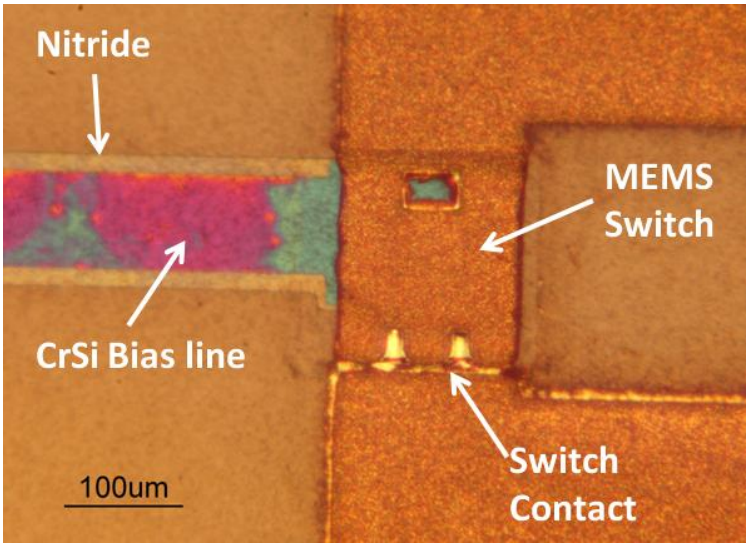



Figure 99: View of a single ohmic contact MEMS switch.

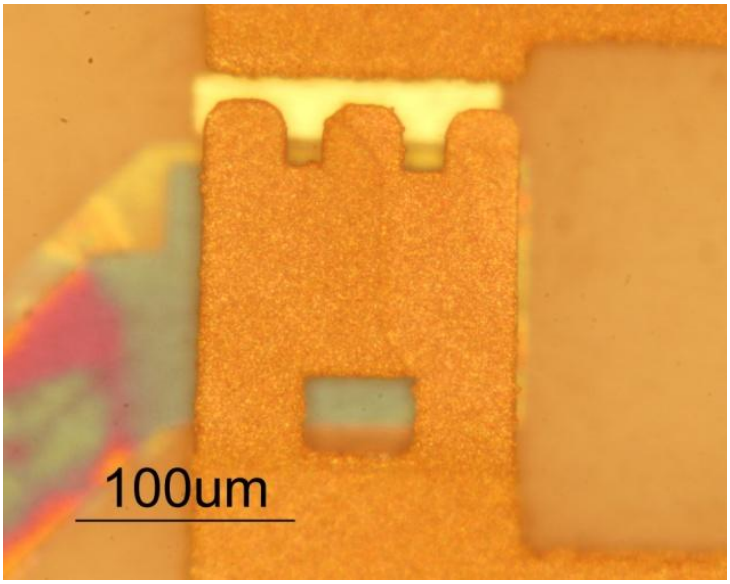



Figure 100: Close up view of the RF MEMS switch.

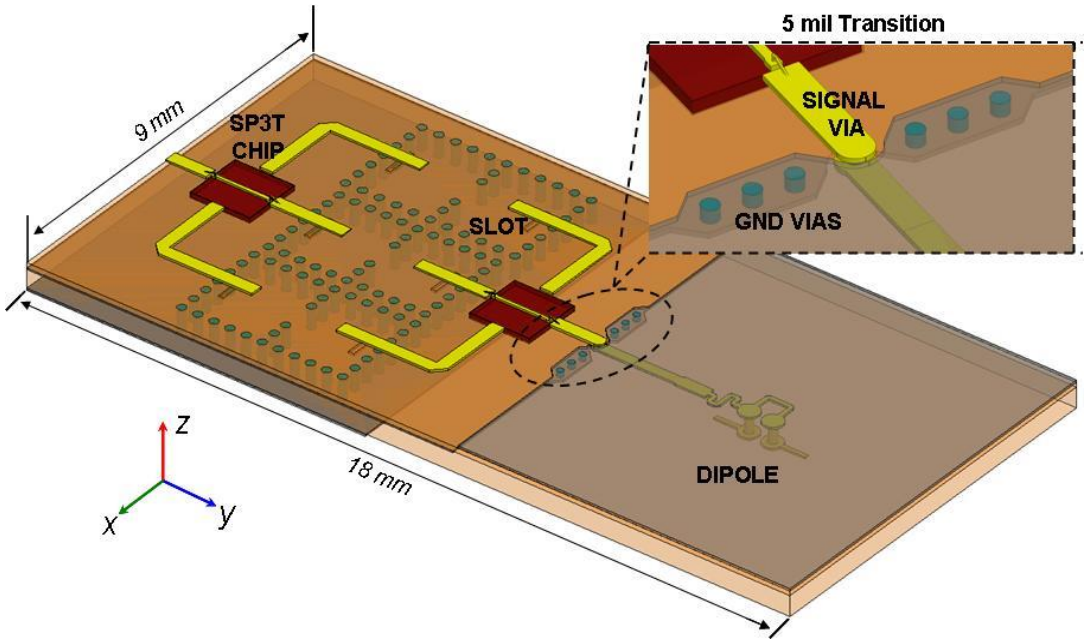
A monolithically integrated reconfigurable antenna using ohmic RF MEMS switches is presented. The integration of the switches directly on LCP minimizes the interference with the antenna pattern. Multilayer LCP is used to create a stack patch design while the MEMS switches that fit in a small gap enable beam steering capability. Accurate alignment for assembly and measurement of the antenna remains as a challenge.

# APPENDIX B

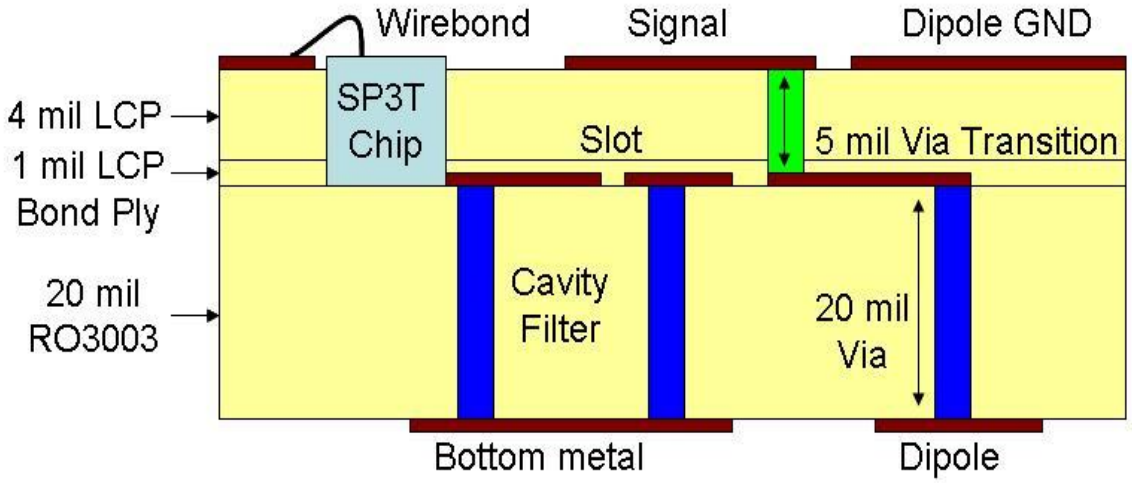
# MM-WAVE RECONFIGURABLE ANTENNA

In this chapter, a reconfigurable filter and antenna is presented at the 60 GHz band. The high frequency band promises over 1 Gb/s data rate over a short distance and enables highly compact and miniaturized systems. However, the design becomes more sensitive to errors from fabrication tolerances that can degrade the system performance drastically. In an effort to reduce these negative effects, a SOP approach is presented to integrate a band selective cavity filter and a vertical dipole antenna. This compact integration solution uses the previously investigated via technology and bonding of LCP.

The overall design of the integrated system is shown in Figure 101(a) which shows the layout of the simulated band selective filter and a vertical dipole antenna with a total dimension of 9 mm x 18 mm. The 3D stack up is shown in Figure 101 (b), where a 4 mil LCP layer is bonded to a 20 mil RO3003 layer with a 1 mil LCP bond ply. Rogers® RO3003 is an organic material and has electrical properties similar to LCP with a dielectric constant of 3 and a loss tangent less than 0.003 at 60 GHz. Three slot fed dual pole cavity filters have been designed using 20 mil vias with an 8 mil diameter as metal walls. They are designed to operate in three different bands with approximately 2 GHz of bandwidth. The frequency bands are designed around three of the four 2.16 GHz channels set in the 60 GHz band. A SP3T is used to enable the selection between the three filters. A cavity is drilled so that the cavity depth matches the height of the SP3T chip at 5 mils to minimize the length of the wire bonds, which in turn will reduce unwanted parasitics. In addition, a 5 mil microstrip to microstrip via transition is used to connect the output of the filter to the embedded feed line of the dipole antenna. The feed line is connected to the dipole, which is on the bottom of the 20 mil RO3003 layer, through 8 mil wide 20 mil tall vias. The vertical stack up allows the ground to be beneath




(a)



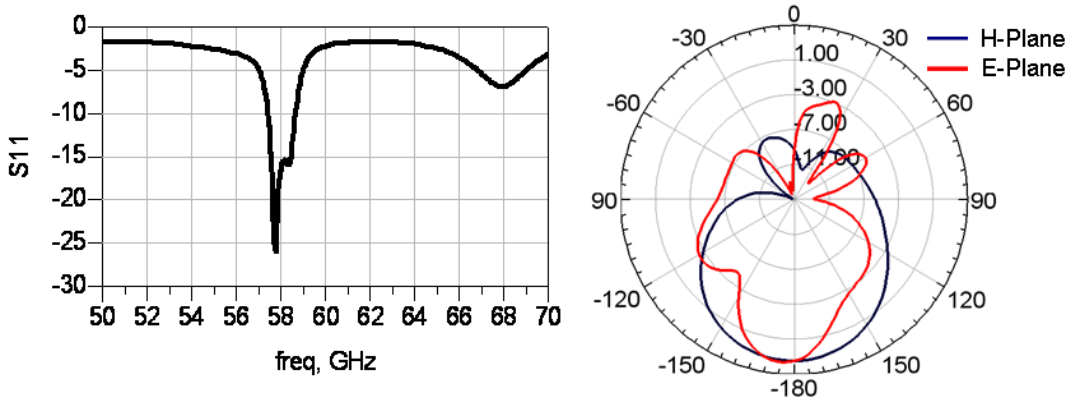

(b)

Figure 101: (a) Layout of the integrated band selective filter and the vertical dipole antenna and (b) the cross-sectional view.

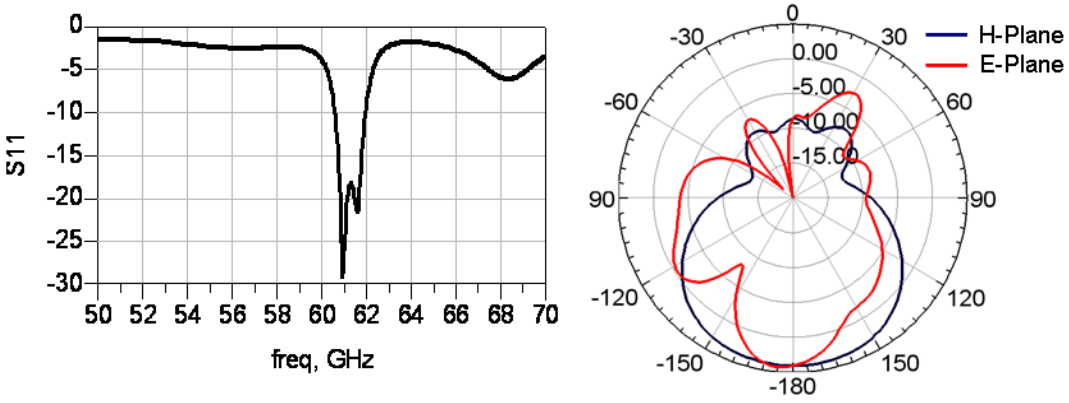
the dipole and by image theory, a higher gain is achievable [78]. In addition, there is less interference from the feed line as it is embedded and the vertical stack up makes it easier for expanding the antenna to an array.

The return loss and radiation pattern of the overall system including the filter, via transition, and the dipole antenna is shown in Figure 101. The $S_{11}$ response shown in Figure 102 (a) shows the first band around 58 GHz and the antenna pattern gives a peak total gain of 3.6 dBi at 57.7 GHz. Figure 102 (b) shows the middle band response around 61 GHz and a maximum gain of 4.2 dBi at 61.2 GHz. Figure 102 (c) shows the upper band response around 64 GHz with a maximum gain of 4.1 dBi at 64.1 GHz for the total system. The gain drop is evident compared to a single dipole as the filter, via transition, and extra line length adds to the loss and shifts the $S_{11}$ response slightly. In addition, the E-plane pattern is distorted significantly as the presence of the filter interferes with the radiation of the dipole.

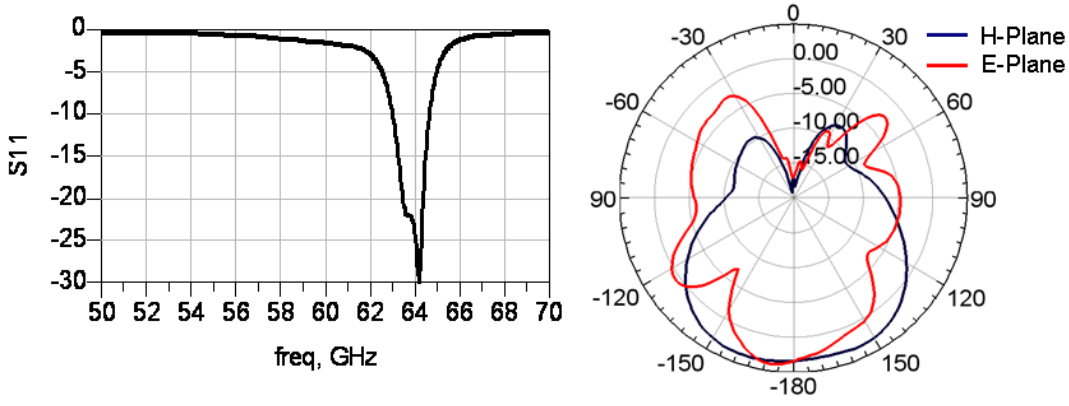
The design of a 60 GHz band reconfigurable filter and antenna is presented on a multilayer LCP platform. The results show the possibilities and advantages of integration on LCP for high frequency SOP applications. The fabrication challenge remains as accurate placement of high aspect ratio vias are required in the multilayer stack up.




(a)




(b)




(c)

Figure 102: Simulated results of the filter and antenna system showing $S_{11}$ and the antenna patterns at (a) 57.7 GHz (b) 61.2 GHz (c) 64.1 GHz.

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